Toward User-Friendly Integrated Circuits
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Invited Speech

解説

Dataquest が主催する半導体産業会議が箱根で開かれた時の講演である。スピーチは日本語で行われたが、資料は英語で作るのが決まりであった。
1986年はその前年から始まったメモリー不況が続き、世界中の半導体メーカーが総じて苦境に陥っていた年である。インテルは85年にDRAMから撤退しており、同年に米国のSIA（半導体産業協会）は日本メーカーをダンピング容疑で提訴した。両国政府間での協議の結果、86年には日米半導体協定が結ばれたのである。

メモリーやマイコンなどの標準品・汎用品中心のビジネスから顧客志向ビジネスへの模索が始まっていた。User-Friendly IC（UFIC)もそのような状況における一つのコンセプトとして提唱されたものである。ユーザーのニーズに適合した製品を、なるべく早い納期で、妥当な価格で納入するというのが基本的な考え方である。その代表事例として日立が製品化を始めたZTATマイコンを取り上げた。ZTATは「TATがゼロ」の意味。

結果として、UFICという言葉が業界で定着することはなかった。その直接的な原因は、日立の海外のマーケティング部門から「UFICという言葉はネイティブスピーカーにとっては語感が悪い」というアピールがあり、使うことを止めたからである。また、このコンセプト自体は翌年（87年）に着想した「牧本ウエーブ」の中に吸収される形となった。
一方、ZTATの方は「Field Programmable」の代名詞のような感じで、この後も長く使われ、今日のフラッシュ・オンチップ・マイコンの先駆けとなった。

なお、この資料は紙ベースでの記録をデジタル化したので、読みづらい箇所が散見される。特にコンマとピリオドが判然としない箇所が多いが、文脈からの判断をお願いしたい。

本文および図面に続く

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TOWARD USER-FRIENDLY INTEGRATED CIRCUITS

Tsugio Makimoto
General Manager
Musashi Works, Semiconductor and IC Division
Hitachi, Ltd.

Dr. Makimoto is General Manager of the Musashi Works, Semiconductor and IC Division, of Hitachi, Ltd. His current responsibilities include all MOS operations, including microprocessors, memories, and ASICs. He has been with Hitachi since 1959. Dr. Makimoto received a B.S. degree in Applied Physics from the University of Tokyo, an M.S. degree in Electrical Engineering from Stanford University, and a Ph.D. from the University of Tokyo.

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1290 Ridder Park Drive, San Jose, CA 95131-2398, (408) 971-9000 Telex 171973

講演が行われた1986年4月は、私が日立半導体の主力工場である武蔵工場・工場長に就任してから間もなくのことであった。前年から続くメモリー不況から如何に脱していくかのシナリオが求められていたのである。そのような状況を背景にして、時代の変わり目における技術・マーケティング戦略を論じたものである。ここで新しく提唱したのがユーザー・フレンドリーIC（UFIC）であり、その代表製品がZTATマイコンであった。

1. Movement towards User-friendly Circuitry

Recent years have seen the appearance of a variety of words to describe semiconductor products aimed at specific user or application needs. One such expression is ASICs, short for application-specific integrated circuits, which was first coined by Dataquest, Inc. There are, however, several other terms in use, as can be seen from Fig. 1.

Looking at this list, there seem to be many differences of nuance from expression to expression; yet, there also seems to be a common thread tying them together. In each case, the designer, manufacturer, or whomever, seems to be aiming at what could be called user-friendly integrated circuits, or UFICs. Again, though, this UFICs term itself is not something that can be defined in great detail, but is rather only indicative of a broad current.

Over the past decade, the semiconductor industry has been predominantly geared toward producing high-performance and highly functional, yet standard, microprocessor and memory devices. The next ten years look to be a UFICs decade, however, with quite a few such devices already proposed or realized. Many more more-sophisticated UFICs are sure to appear in the very near future (see Fig. 2).

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1. ユーザー・フレンドリーICに向けての動き

近年、顧客志向を目指す製品の新語が多く見られる(図1参照)。Dataquest 社の造語であるASICもその一つである。このような新語は全体としてUser Friendly IC(UFIC)という言葉にまとめられよう。これまでの10年はMPUとメモリが半導体の主流を占めていたが、これから次の10年はUFICの時代になるだろう。すでにいくつかのUFICが出ているが、これからさらに多くのものが出てくるだろう。それは顧客ニーズに合致し、コスト性能比に優れ、しかもTATの短い製品群である。

No matter what the UFIC. though. it will need to display high performance and sophisticated functions. Moreover. it will need to meet extremely specialized customer needs. And. it will need to do so in a way guaranteed to minimize necessary lead time to the greatest possible extent.

2. Why UFICs?

Tremendous improvements in user systems have been the result of the ongoing advances being made in semiconductor technologies. One major area of progress is in decreasing the number of required system componenents (Fig. 3). A particularly appropriate example is hand-held calculators. because of the important role they have played in driving early-stage MOS development.

Progress has been remarkable. Early on. these calculators made use of thousands of transistors and diodes. With advances in IC technology. the number of components was then reduced to 2-300. Moving on to the LSI era. it has finally became possible to configure the entire calculator circuitry from only a single chip. What is more. major improvements have also been registered in ease of function execution. power consumption and a variety of other areas during this same period. Current state-of-the-art is a calculator with virtually the same dimensions as a business card.

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2. なぜUFICに向かうのか

半導体技術の進展によって電子システムは大幅な進歩を遂げてきた。特に大きな進歩は部品点数の低減であり、中でも電卓の進歩は極めて顕著な事例である(図3)。当初数千個にも及んだ部品点数は、今日ではワンチップLSIとなり、名刺サイズの電卓が実現されている。

Advances in IC integration are also playing a major role in reducing the number of necessary components in many other types of systems and equipment (see Fig. 4). Looking at TVs, the early 1970s saw a one order drop from the need for hundreds of transistors and diodes to the need for tens of them. At the present, television sets are being manufactured with use only of a few ICs or LSIs and a few tens of transistors and diodes. Progress in the facsimile terminal area also is remarkable. Again, hundreds of ICs were required early in this decade. Now, however, sets are coming out that embody only a few tens of such integrated circuits.

The advances referred to in semiconductor technologies have come together with progress in other areas to facilitate development of so many sophisticated and convenient equipment systems that could not even have been envisioned only a few years ago. Whether in the form of personal computers or auto-focussing cameras, supercomputers or digital telecommunications switching equipment, industrial robots or what have you, examples are almost too numerous to name. Semiconductor technology progress has supported reduced costs and expanded applications in systems making use of ICs, thus in turn contributing to a huge expansion in demand for the very same semiconductor devices. This explosion of demand has itself provided the driving force for further technological leaps, thus working out very symmetrically.

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ICの進歩によって、電卓以外でも多くの電子機器の部品点数が低減されてきた(図4)。テレビでは数百点もあった部品が数十までに低下した。ファクシミリでも同様である。
さらに半導体の進歩によって、これまで想像すらできなかった製品が出回っている。たとえば、パソコン、自動焦点カメラ、スパコン、デジタル交換機、産業用ロボットなど枚挙にいとまがない。半導体の進歩は電子機器のコスト低減をもたらし、大きな需要を生み出した。その結果、半導体技術はますます発展し、相乗的な効果を生み出している。

New types of semiconductor products are, however, becoming necessary as a result of these trends toward greater integration and expanded application areas (see Fig. 5). The application system designers and manufacturers making use of such devices are faced with developing and marketing systems that not only fit the needs of end-users to the greatest possible extent, but that also display some distinguishing difference from those systems put out by their competitors. When ICs were not so highly integrated it was possible to provide such distinguishing characteristics through unique arrangements of standard LSIs. In this time of VLSIs and UlSIs, however, such arrangements have to be made on the actual chips themselves. Applied system developers accordingly need chips that match the systems they are in the process of putting together.

Looked at from the semiconductor manufacturer side of things, there are other problems arising in this period of increasingly greater integration. Leaving aside the general-purpose megabi memories and high-end microprocessors now becoming possible for the first time, the combination on a single chip of 4/8 bit CPUs and peripheral ICs that used to be individual chips in themselves has thrown into danger the whole general-purpose nature of such LSIs. At this juncture, UFICs look to have a major role to play in dealing with the problems faced by both application system developers and semiconductor manufacturers.

Based on the discussion above (see Fig. 6), UFICs can possibly be defined as devices that will facilitate movement from a user's

集積度の増大によって半導体のユーザー・メーカーともに大きな課題に直面している(図5)。機器のメーカーはエンドユーザーのニーズに応えるとともに、コンペチタとの差別化を図らねばならない。以前は小規模ICの組み合わせによってこれを可能にしたが、これからはチップ自体での対応が必要となる。半導体メーカーにとっては、小規模デバイスは汎用性があったが、集積度の増大と共に汎用性は失われる。UFICはシステム・コンセプトから実装に至るTATを最短にすることを目指すデバイスであり、機器メーカー、半導体メーカーの双方にとって進むべき方向だといえる(図6)。

system concept to implementation of the actual system in the shortest possible amount of time--that is. realization of the quickest possible turn around time.

Considering any system to fundamentally consist of both hard and software. two things look to be of increasingly greater importance in the software area: supply of sophisticated support tools that will speed-up software development by the user. and provision of field programmable LSIs that will facilitate the quickest possible writing into the device of the developed software. In the hardware area the key appears to be how to get the chips fitted to the needs of the particular user to him in the shortest possible amount of time. Here. design automation. or DA. has a vital role to play. This DA also needs to be capable of dealing with the problem of testability that is becoming increasingly more intractible as integration scale increases.

3. Underlying UFICs Technologies

3.1 Field-programmable Devices

There are two approaches to making the dedicated ICs that users now require (Fig. 7). First is by manufacturing mask-programmable devices. or MPDs for short. and the second via production of field-programmable devices. or FPDs. MPDs are customized during the wafer manufacturing process through use of

2. （続き）
システム設計はハードとソフトの両面で行われるが、ソフトの面ではサポート・ツールの提供とプログラマビリティーが重要。ハードの面ではDAとテスタビリティが重要である。

3. UFICの基盤となる技術
ユーザー向けに特化したICを作るには二つの方法がある（図7）。その一つはマスク・プログラマブル・デバイス（MPD）であり、もう一つはフィールド・プログラマブル・デバイス（FPD）である。

hot masks designed to fit each particular device. Representative examples are mask ROMs and gate arrays. FPDs are LSIs where. after purchase from the manufacturer. the user can employ support-tool programmers to write-in software of his own specification. Examples here are electrically programmable ROMs. or EPROMs. and programmable logic devices. or PLDs.

With MPDs. it takes approximately one month or more before samples can be shipped to the user after an order has been received by the manufacturer. Because the user himself can undertake programming in a most simple manner with FPDs. however. turn-around time, or TAT. is reduced to virtually zero. Accordingly. FPDs can be labeled as being quite user-friendly.

Field-programmability would thus look to be a basic UFICs technology. Let's take a look. here. at an example.

Hitachi's ZTAT microprocessor is a plastic packaged microcomputer with a built-in EPROM. Compared to conventional single-chip microprocessors with internalized mask ROMs. this ZTAT facilitates a multitude of benefits. including:

1. ROM programming with a turn-around time of zero:
2. little risk of software bugs because there is no need for the user to order out his ROM programming: and
3. optimal suitability as a bridge to future mass production through use of later-developed masks (quick mass-production startup is possible and user opinions

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MPDの代表的な事例はマスクROM とゲイトアレイであり、受注してから出荷までは一月ほどもかかる。一方、FPDの事例はEPROMとPLDであり、ユーザーが自分でプログラムを書き込める。TATはゼロに近く、極めてユーザー・フレンドリーであるといえる。
日立のZTATマイコンはプラスティック・パッケージ版のEPROM 内臓マイコンであり、次のような利点を持つ。1)書き込みのTATはゼロ、2)ROMコードのバグに伴うリスクが少ない、3)マスク版による量産品へのつなぎとして最適(ZTAT版でエンドユーザーの声を聞いてからROMコードを固定することが可能)。

can be received and responded to before beginning mass production).

Development of this advanced type of device became possible upon consolidation of the several underlying technologies (refer also to Fig. 8):

1. high-performance microprocessor architecture;
2. CMOS EPROM techniques;
3. chip passivation to insure increased reliability, as well as plastic packaging techniques; and
4. highly efficient testing techniques for EPROMs and microcomputers accomodated together on the same chip.

Single-chip microprocessors with quick TATs were available before the advent of this ZTAT microcomputer (Fig. 9). However, comparing the ZTAT to conventional single-chip microprocessors with built-in mask ROMs should provide a clearer understanding of the advantages provided by this new device.

Microprocessors with internalized mask ROMS do provide economicality, yet the TAT needed for ROM programming is a problem. To achieve a quicker TAT, the piggy-back configuration made an appearance. What this entails is making it possible to place a commercial EPROM on the back of a microprocessor package. A virtually zero TAT could be achieved, but price problems appeared with this configuration. Microprocessors with built-in EPROMS accordingly next appeared on the scene. Because these were ultraviolet erasable PROMs, windows had to be equipped in

ZTATマイコンを可能にするためには次のような技術が必要であった。1)高性能マイコン・アーキテクチャー、2)CMOS版のEPROM技術、 3)信頼性確保のためのパシベーション技術とプラスチック・パッケージ技術、4)PROM混載マイコンの効果的なテスト法。
ZTATに至るまでの各種アプローチを示す(図9)。マスクROM搭載マイコンは経済性は高いが、TATが長いのが問題。パッケージの上に市販のEPROMを背負ったピギーバック版はTATはゼロであるが、コストが高いのが玉に傷。窓付きEPROMオンチップ版もコストが高かった。

the packages. This made it impossible to drop prices down to suitable levels.

Finally, we come to development of the ZTAT. In appearance it looks the same as a conventional mask ROM, while the price is also close.

Let's look at what kind of applications have become possible as a result of development of this ZTAT (see Fig. 10). In the past there was little need to change the software to be written into a ROM. Moreover, mask ROM devices have been employed for applications where large numbers of chips are required. On the other hand, when the frequency of changes to software was high and the volume needed low, window-type microcomputers have been employed. In respect to intermediary applications, however, use of mask ROMs carries with it a risk, while use of window-type devices is expensive, thus facing the user with a dilemma.

ZTAT devices are ideal single-chip microprocessors for plugging this gap. The user can employ any number of chips whenever and wherever he desires. As you can see, then, UFICs aims have been advanced.

3.2 Electrically Erasable PROM (EEPROM) Technology

In comparison to EPROMs which are erasable with applied use of ultraviolet light, EEPROMs are PROMs which can be written and

ZTAによってどのような応用分野が開けたかを示す（図10）。これまでROMコードが固定した大量生産品にはマスクROM版が使われ、書き換え頻度が高く、少量生産の場合には窓付きマイコンが使われてきた。中量生産品についてはマスク版ではリスクを伴い、窓付き版ではコストが高いというディレンマがあった。この隙間を埋めるのがZTAT版である。

3．2 電気的に消去可能なPROM(EEPROM)

erased electrically. Though EEPROMs are larger than EPROMs, they offer major advantages in that a windowed package does not need to be employed and that programs can be written into them and changed even after the devices are assembled into a system. EEPROMs are accordingly a prime candidate for UFIC status.

EEPROMs have a long history (see Fig. 11). Only now, however, have 64 k-bit level devices come onto the market. Compared to the 16 k-bit circuits of only a few years ago, these now offer such advantages as:

1. a single, 5 V power supply rather than the previous dual source;
2. variable widths (byte-wide as well as chip-wide) for programming and erasure, greatly quickening these two activities;
3. high-speed operation; and
4. built-in circuitry that was formerly on peripheral devices.

The 64 k-bit devices are accordingly a lot easier to use.

Let's look a little more closely at these technological trends (Fig. 12). The cell area needed for one bit of EEPROM memory differs according to process resolution. At the same resolution, however, EEPROMs fall midway between DRAMs and SRAMs. In other words, while EEPROMs require two transistors per single bit of memory, DRAMs take one and SRAMs (in the Hitachi case) need four plus two resistors.

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3．2電気的に消去可能なPROM（EEPROM）

EEPROMではROMの中身は電気的に消去可能であるから、システムに組み込まれた後でもコードを書き換えることができる。消去に紫外線を必要とするEPROMとは大きな違いがあり、UFICの有力な担い手となろう。

EEPROMは長い歴史を持つ（図11）。現在やっと64Kビット製品が出たばかりだ。しかし、16K品に比べれば多くのメリットがあり、使いやすくなっている。技術のトレンドを見てみよう（図12）。

Taking Hitachi's EEPROMs as an example (see Fig. 13), cell size has tended to shrink to one fourth over a five year period. This has been accomplished not only by employing processes with finer line resolution but also by making use of a three-dimensional configuration (a tri-gate structure) for the two transistors needed for each bit.

There are two main technologies employed for EEPROMs: MNOS (or metal nitride oxide semiconductor), and floating gate (see Fig. 14). Each has its strengths and weaknesses; in short, MNOS provides a structure that is in principle simple, while the floating gate process is compatible with that for conventional EPROMs.

One current trend is to load an EEPROM on-chip. One such example can be seen in Fig. 15. This is an 8-bit microcomputer realized via a 2 um CMOS EEPROM process that provides, on-chip, 3 k-bytes of ROM, 128 bytes of RAM and a 2 k-byte EEPROM. A protection circuit is also provided which prevents external reading of written data without use of a stipulated procedure.

Sample applications (see Fig. 16) for just such a microprocessor with internalized EEPROM include:

1. individualized information registry taking the form of, for example, a credit or ID-type IC card;
2. precision machinery systems requiring fine adjustments: and

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日立の製品の場合、メモリセルのサイズは5年で1／4に縮小した（図13）。これは微細化に加えて、3次元のトライゲート構造を採用したからである。EEPROMの構造にはMNOS型とフローティング・ゲート型がある。前者は構造がシンプルであり、後者は通常のEPROMプロセスと互換性を持つことが特徴。最近ではEEPROMを混載する傾向もでているが、8ビットマイコンの事例を示す（図15）。
このマイコンによって可能となる応用の事例を示す（図16）。例えば、IDやICカードなどへの個別情報の書きこみ、精密機械の微調整、遠隔地にある装置のソフトウエアのアップデイトなど。

3. updating of software used in remote equipment.

Field programmability is, in this way, serving to meet the most minute user needs. Moreover, it is likely to be subjected to even further development in the future as a central UFICs technology.

3.3 Chip Design Automation

One fundamental UFICs feature involves getting the dedicated chip the user needs to him as fast as possible, as has already been mentioned (see Fig. 17). What this actually entails, however, is streamlining as well as fully automating the process from system to chip design.

In the days when integration density was not so great, it was possible for designers to manually put together circuits even when the logic was somewhat random or arbitrary. At the present day, however, where hundreds of thousands of transistors are being put onto one chip and the circuit diagram has become something several square meters in area, it is getting extremely difficult to do things manually. Disciplined design with DA backup is now becoming a vital requirement. What this "disciplined" design signifies is the modularization of logic, and structuring of the circuitry by means of a modular assembly approach. DA then involves automatic module design or automatic design of chips combining these logical modules.

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3.3 チップ設計の自動化

UFICで大事なポイントはユーザー向けチップを最短の時間で顧客に届けることである(図17)。集積度が高くなかった時代にはマニュアル設計でもよかったが、今日の数十万個のトランジスタが搭載されるチップではマニュアルでの対応は困難である。論理回路のモジュラー化を前提にし、DAによる正則的な設計が必須となる。

The ultimate goal of DA is development of the necessary tools that make it possible to input the system concept and merely wait for the output of a silicon chip (see Fig. 18). Automatic design techniques are now being established for each stage from system to chip design. Accordingly, problems for solution in the near future are integration of each of these techniques in a total, overall process as well as automated realization of chips that compare favorably with manually designed chips in terms of chip size and performance.

With establishment of the optimal DA system as envisioned today (see Fig. 19), all the designer will need to do is describe system functions in a high-level language and confirm simulation results to realize a fully designed dedicated chip. The DA system will then undertake generation of a logical diagram from the input functions, generation of the necessary cells, layout of the overall chip through combination of these cells, and output of the data necessary for fabrication of the required hot mask. Simultaneously, a test pattern for confirmation of the suitability, etc. of the fabricated LSI will be automatically generated.

Currently, there are several ways to go about realizing dedicated LSIs (Fig. 20). These include a full-custom, standard cell, gate array, and PLD approach. In each case, the TAT and chip size characteristically differ. With the UFICs goal being minimum chip size with minimum turn-around time, it is apparent that a major DA system advance is now needed.

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DAの究極の姿はシステム・コンセプトを入力すればチップが自動的に出てくることだ。現在では設計の各段階での自動化に留まっており、その統合が必要だ。そのようなシステムができれば、設計者のすることは、高レベル言語でシステム機能を記述し、シミュレーション結果を確認することである(図19)。DAシステムではこれを基にしてマスク製造のためのデータを作り、さらにテストパターンを出力する。専用LSIを作るには四つのアプローチがある(図20)。各々のアプローチによってTATとチップサイズは大きく異なるが、UFICの狙いは最短のTATと最小のチップサイズを実現することにある。

3.4 Testability

Unfortunately, 100% of all manufactured semiconductors do not end up meeting original quality objectives (see Fig. 21). Accordingly, some kind of test is necessary for the culling out of defective products. One unfortunate result of the recent trend toward increasedly dense LSIs, however, is that chip testability has markedly decreased.

Just what signal strings will be output with input of just what signal strings--what is known as the test pattern is the series of signal strings that makes this determination possible. "Fault coverage" is a unit of measurement clarifying to what extent defects appearing in LSI circuitry can be detected. Comparing test pattern fault detection rates with the percentage of defective devices found among good quality devices at each sorting, it can be seen that the test pattern fault detection rate needs to be at least 90-95% for assurance of reasonable quality.

However, manpower required for realization of this 90-95% goal via use of fault simulators tends to increase greatly with LSI integration scale (see Fig. 22). This is because the number of places where defects may occur increase proporionately to the density of the circuit, and it accordingly becomes more difficult to monitor all such locations within the chip from "outside" the chip. Not only, then, is automatic design of the chip important.

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3.4 テスタビリティ

製品はすべて良品とは限らないので、何らかのテストが必要であるが、集積度の増大とともに、十分なテストができなくなっている。よい品質を確保するには、欠陥の検出率は最低でも90～95%程度は必要である。しかし、集積度の増大に伴って、このようなレベルを人手で達成することは大変難しくなっている（図22）。設計の自動化のみならず、テスト・パターンの自動生成が必要になっているのだ。

but another vital requirement is automatic generation of the above-mentioned test patterns.

Let's take a look at one method of automatic test pattern generation (Fig. 23). With automatic addition of a test circuit covering all flipflops in any user logic circuit, it becomes possible to freely conduct flipflops and to read and write data from outside the LSI. Employment of this technique assures relatively simple automatic test pattern generation no matter how complex the chip.

5. Conclusions

"Systems on chip" have already begun to appear in calculator and watch applications. Semiconductor progress is sure to make it possible to realize other large-scale systems on a single chip. Depending on the application it will become necessary not only to integrate the CPU, memory and similar digital circuitry but also analog circuits on the same chip.

The UFICs that have been discussed in this paper are aimed at assuring that the user can freely combine a wide variety of semiconductor circuitry, with it ultimately becoming possible to mount it all on a single chip. Moreover, it must be possible to do this with minimum TAT, and within a minimum chip size. Once such devices make an appearance, it will become possible to offer truly friendly systems to end users, and to greatly improve the

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自動的にテストを生成する方法の一つを紹介する(図23)。それはすべてのフリップフロップをカバーするテスト回路を挿入する方法であり、複雑なLSIでも自動的にパターンを生成することが容易になる。

5. 結論

電卓や時計では、すでに“システムオンチップ“が現実になっている。この傾向は広がって行くだろう。UFICの狙いはユーザーにとって必要なあらゆる回路を一つのチップに集積することであり、それを最小のTATと最小のチップサイズで実現することである。

human/machine interface.

TOWARD
USER-FRIENDLY INTEGRATED CIRCUITS

T. MAKIMOTO
MUSASHI WORKS
HITACHI, LTD.

ASIC : Application Specific IC
- Gate Array
  - Structured Array
- Standard Cell
  - Super Integration
- Programmable Logic Device (PLD)
  - Programmable Array Logic (PAL)

ASSP : Application Specific Standard Product
- Video RAM

ZTAT : Zero Turn Around Time

Fig. 1 UFICs RELATED TERMINOLOGY

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ユーザーフレンドリーICに向けて

日立製作所　武蔵工場
牧本次生

図1　UFICに関連した言葉

比較的新しく出てきた用語を並べて、単なる標準品・汎用品の時代からカスタム指向に変わりつつあることを示している。ASICはDataquestの造語であり、ZTATは日立の商用語である。

SUPERIOR COST PERFORMANCE
SOPHISTICATED FUNCTIONS

+

SPECIALIZED CUSTOMER NEEDS
QUICK TAT

Fig. 2 UFICs REQUIREMENT

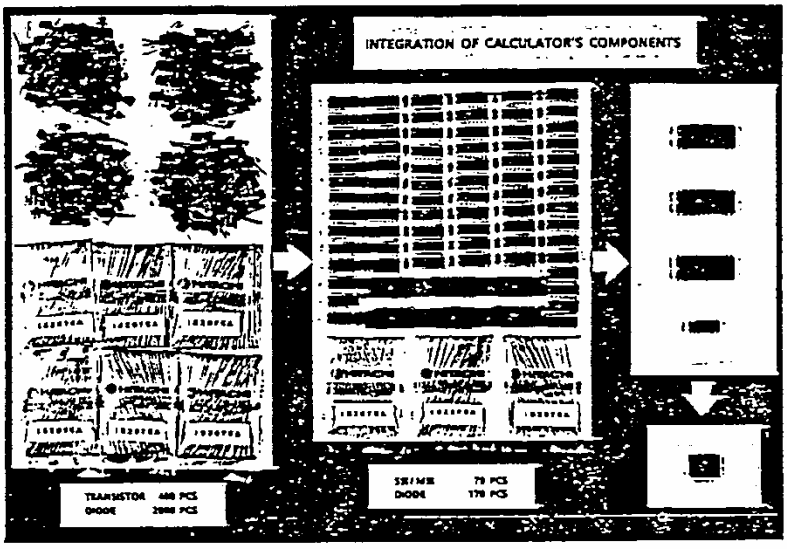

Fig. 3 INTEGRATION OF CALCULATOR'S COMPONENTS

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図2 UFICの必要条件
「複雑な機能を優れたコスト性能比で実現すること」及び「顧客の特定ニーズに応え、これを短いTATで実現すること」
図3 電卓用部品点数の推移
数千個のトランジスタ・ダイオードからIC,LSIの進歩を経て、現在ではワンチップ化が実現された。

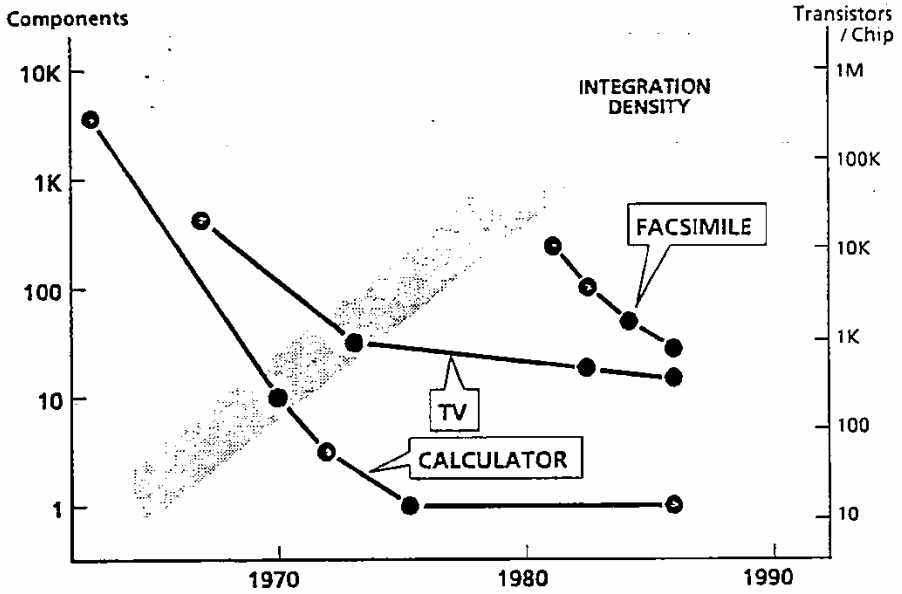

Fig. 4 DRASTIC DECREASE IN NO. OF COMPONENTS

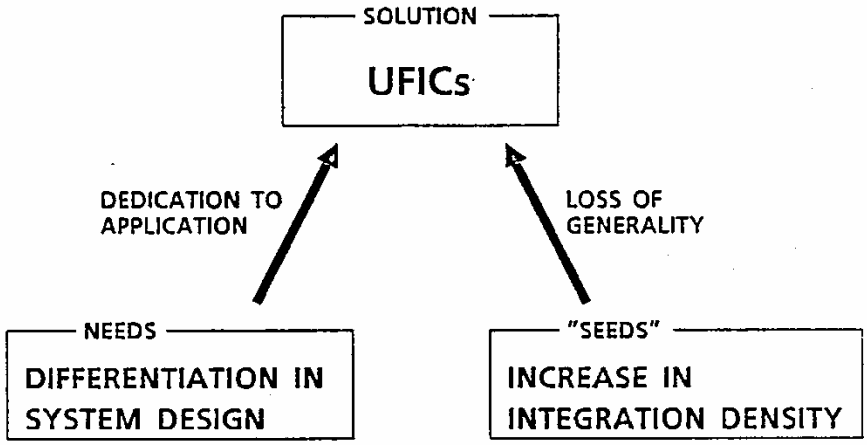

Fig. 5 WHY UFICs

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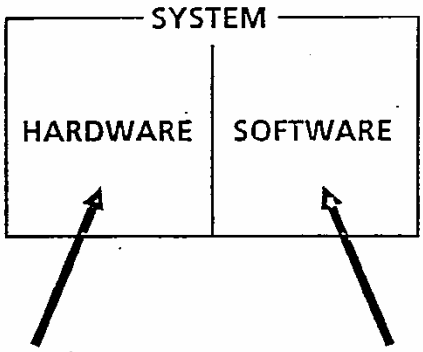
図4 部品点数の劇的な低減
チップの集積度の増大により、電卓では数千の部品点数数が現在では1個になった。TVやファクシミリでも約1／10に減少している。

図5 なぜUFICか
ニーズとしてはシステムの差別化であり、シーズとしては集積度の増大がある。両者がマッチングしたところにUFICがある。



- DESIGN AUTOMATION FOR DEDICATED CHIPS
- TESTABILITY
- SUPPORT TOOLS FOR PROGRAMMING
- FIELD PROGRAMMING

Fig. 6 REQUIREMENTS FOR QUICK TAT FROM CONCEPT TO IMPLEMENTATION

— PLASTIC ENCAPSULATED EPROM ON-CHIP MICROPROCESSOR —

ZTAT OFFERS

- ZERO TURN AROUND TIME FOR MASK PROGRAMMING
- ZERO RISK OF ROM CODE ORDER PROBLEMS
- INTERIM SOLUTION BEFORE MASKED PRODUCT INTRODUCTION

Fig. 7 WHAT IS THE "ZTAT"

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図6 コンセプトから実装に至るTAT短縮の要請

●ハード面では専用チップ向けのDAとテスタビリティー、●ソフト面ではプログラム用のサポート・ツールとフィールド・プログラマビリティーが重要となる。

図7 ZTATとは何か？

プラスティック・パッケージに封入されたEPROMオンチップのマイコンである。特徴は●プログラム作成のTATがゼロ、●ROMコード発注の際のリスクがない、●マスクROM版の生産開始までのつなぎの役割

- HIGH PERFORMANCE MICROPROCESSOR ARCHITECTURE
- CMOS EPROM PROCESS TECHNOLOGY
- RELIABLE PASSIVATION AND PLASTIC PACKAGING
- EFFECTIVE TESTING OF MICROPROCESSOR / EPROM

Fig. 8 TECHNOLOGY UNDERPINNINGS OF ZTAT

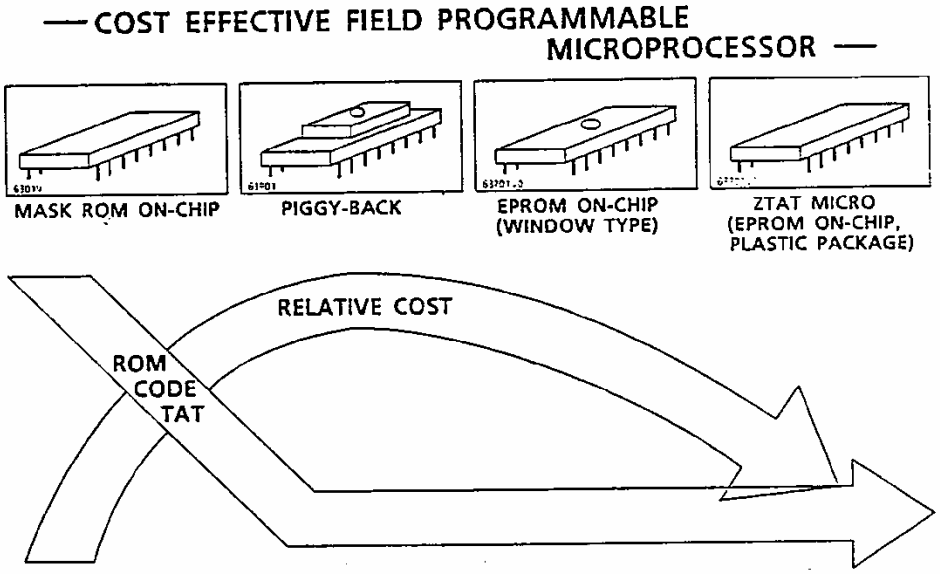

Fig. 9 ZTAT EVOLUTION

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図8 ZTATのための技術基盤
●高性能マイコン・アーキテクチャ、●CMOS EPROMのプロセス技術、●パシベーション技術とプラスティック・パッケージング技術
図9 ZTATに至る流れ
マスクROM版、ピギーバック版、窓付きEPROM版、ZTAT版についてコストの相対比較を示す。
ZTAT版はTATがゼロで、マスクROM版に近いコストの実現を目指す。

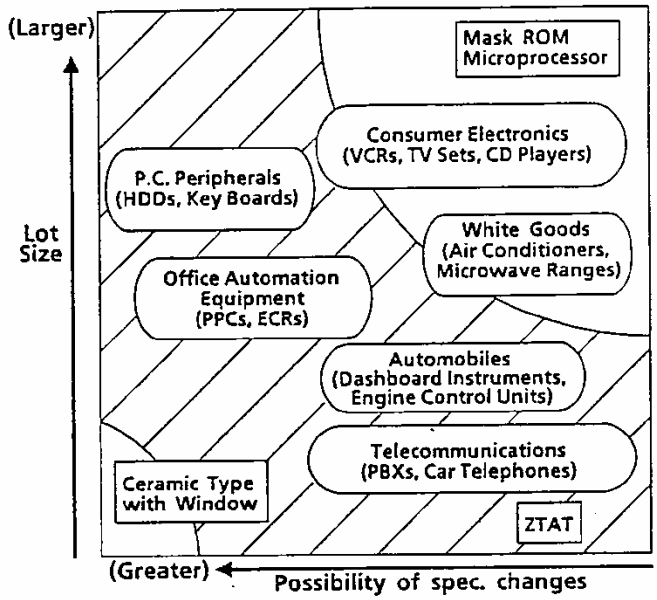

Fig. 10 ZTAT APPLICATION

1979	1985
16K bit (2K×8)	64K bit (8K×8)
3μm N-MOS	2μm C-MOS
Double Power Supply	Single 5V
Chip Erase	Chip / Byte / Page Erase
Byte Write	Byte / Page Write
Read Access Time 350 / 450 ns	200 / 250 ns
Write Time 20 ms	10 ms
	Peripheral Circuits on Chip Address, Data Latches, Data Protection etc.

Fig. 11 EVOLUTION OF EEPROM TECHNOLOGY

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図10 ZTATの応用分野

仕様変更の頻度が低く、数量の大きいものにはマスクROM版、仕様変更頻度が高く数量の小さいものには窓付き版が向いている。中間の分野にはZTATが適す。通信、自動車、OA、PC周辺などを含む。

図11 EEPROM技術の変遷

1979年版と85年版の比較。3μから2μとなり、ビット数は4倍に。性能面でも大きな進歩があった。

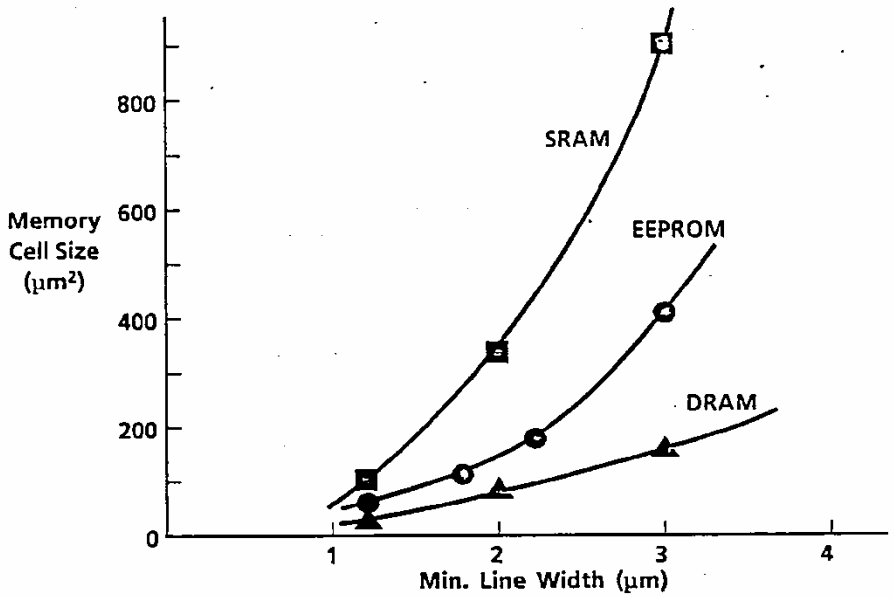

Fig. 12 CELL SIZE FOR MOS MEMORIES

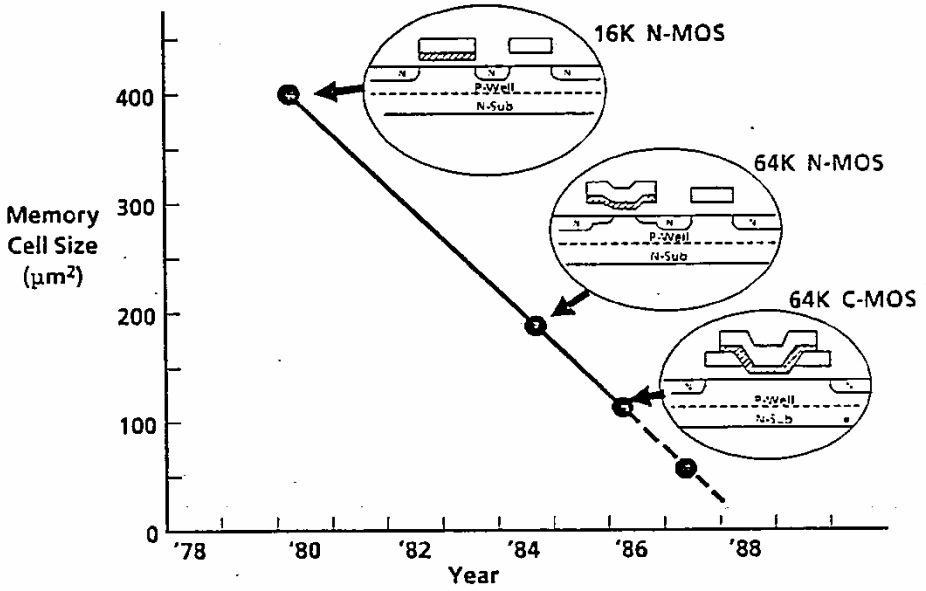

Fig. 13 EEPROM MEMORY CELL SIZE TREND

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図12 メモリのセルサイズの推移
EEPROMのセルサイズはDRAMとSRAMの中間にある。
図13 EEPROMのセルサイズの推移
16K NMOSから64K NMOSへ、さらに64K CMOSに移行するとともにセルサイズは大幅に縮小した。

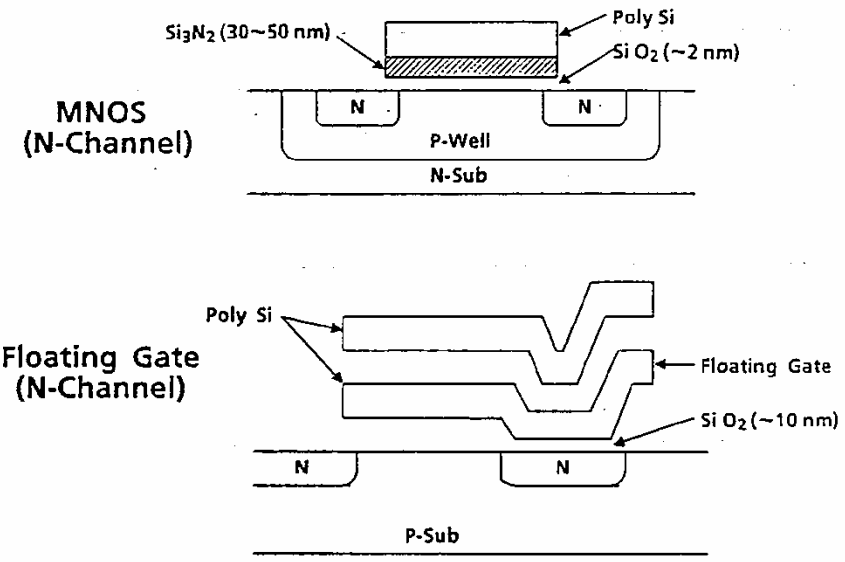

Fig. 14 EEPROM STRUCTURES

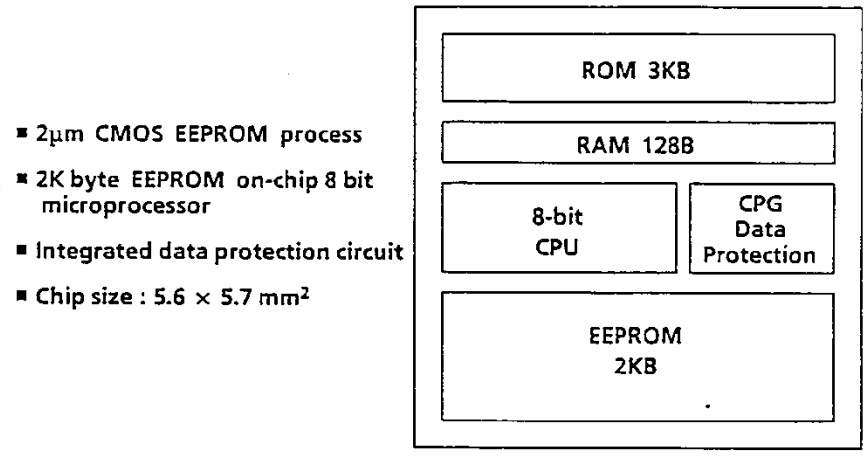

Fig. 15 EEPROM ON CHIP MICROPROCESSOR

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図14 EEPROMのセルの断面構造
フローティング・ゲイト方式とMNOS方式のセルの断面を示す。構造はMNOSの方がシンプルである。
図15 EEPROM搭載のマイコン
2μCMOS EEPROMプロセスをベースにして、2KバイトEEPROMを搭載した8ビット・マイコン。データ保護回路を内蔵している。当時の最先端マイコンの事例である。

Type of Applications	Examples
Personal Information Storage	▪ IC Card (Bank Card, Credit Card etc.) ▪ Security System ▪ ID Card
Data Calibration	▪ TV Tuner Control ▪ Automotive Applications ▪ Robotics, Precision Control
In-Circuit Software Up-date	▪ Remote Controller ▪ Factory Automation

Fig. 16 APPLICATIONS OF EEPROM ON CHIP MICROPROCESSOR

- OVERALL AUTOMATION FROM CONCEPT TO SILICON CHIP

PROBLEMS TO BE SOLVED

- SYSTEM INTEGRATION
- CHIP COMPETIVENESS
  - — CHIP SIZE
  - — PERFORMANCE

Fig. 17 DESIGN AUTOMATION OBJECTIVES

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図16 EEPROM搭載マイコンの応用分野
個人情報保持(銀行カード、クレジットカード、保安システム、IDカード)、データの較正(自動車、ロボット、精密制御機器)、ソフトウエアのアップデイト(遠隔制御、FA)

図17 DAの目標
コンセプトからSiチップまでを一貫自動化すること。解決すべき課題はシステム機能集積とチップの競争力(チップサイズと性能の両立)

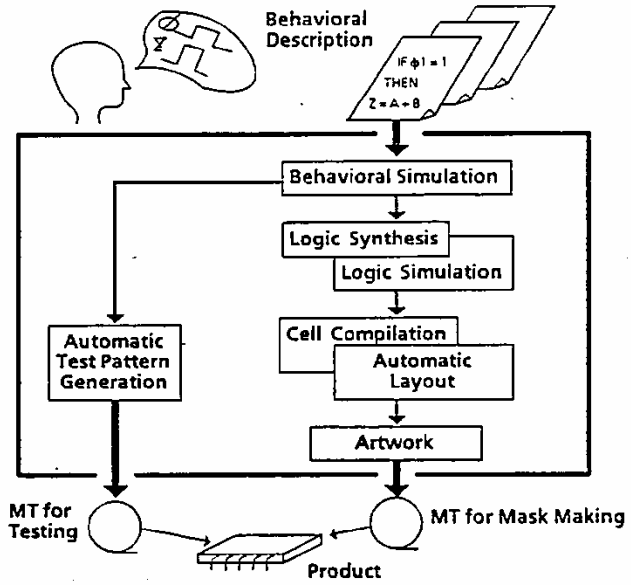

Fig. 18 INTEGRATED DESIGN AUTOMATION SYSTEM

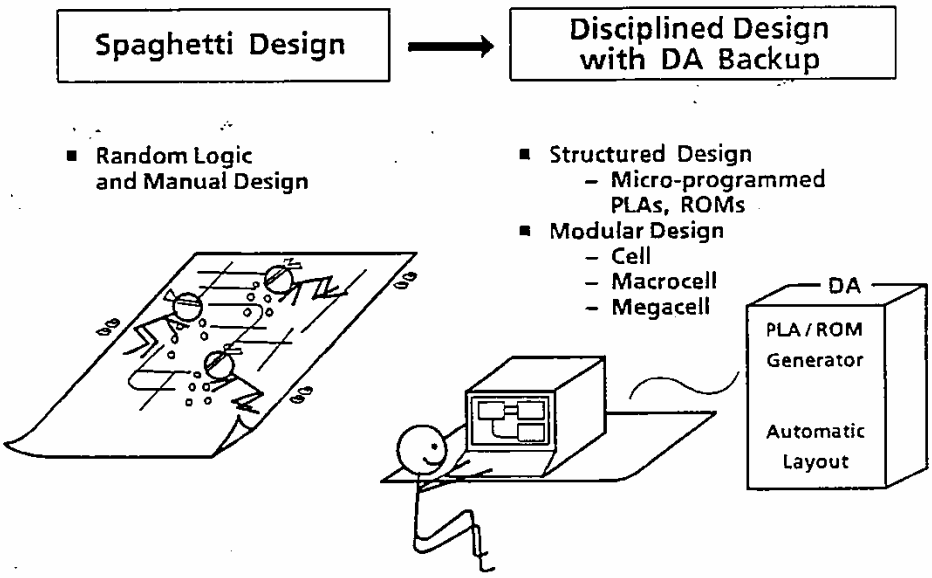

Fig. 19 DESIGN METHODOLOGY

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図18 統合DAシステム
動作記述言語でシステム機能を記述し動作シミュレーションを行う。これをベースにして論理合成、レイアウト設計を行い、マスク作成用のデータを作る。合わせてテストパターンの自動生成を行う。

図19 設計方式
これまではマニュアルで論理回路を設計していた(スパゲッチ設計)、これからはDAを基本にした正則的な設計が必要。マクロセル、メガセルなどの大規模セルを活用することも大事だ。

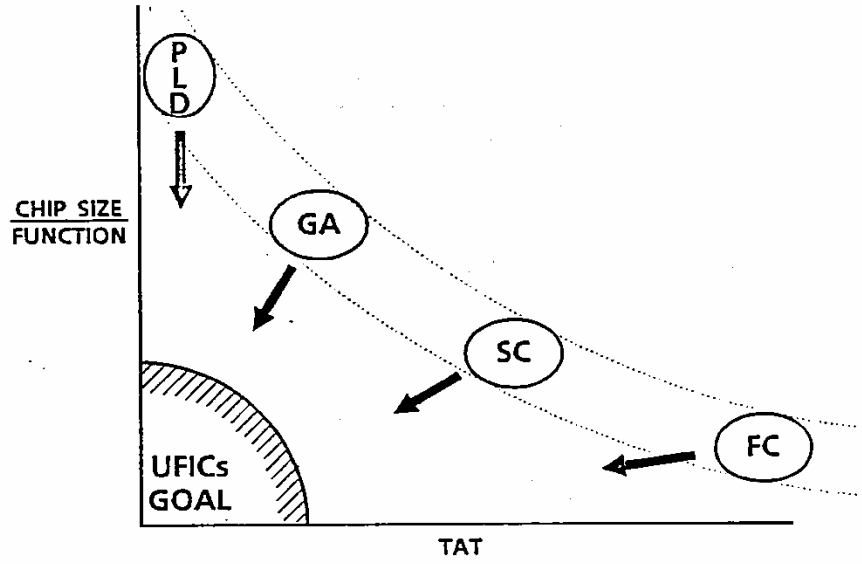

Fig. 20 TRADE-OFF BETWEEN TAT AND CHIP SIZE

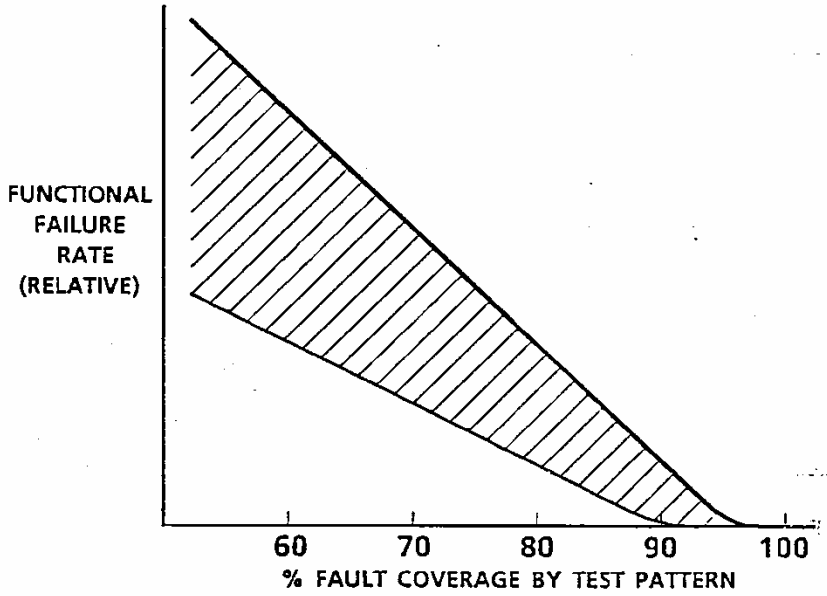

Fig. 21 PROBLEMS CAUSED BY POOR TESTABILITY

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図20 TATとチップサイズのトレードオフ
PLD、ゲイトアレイ(GA)、セミカスタム(SC)、フルカスタム(FC)の各方式についてTATとチップサイズのトレードオフを示す。UFICの狙いは最小のチップサイズと最短のTATの実現である。

図21 テスタビリティーが悪い場合の問題点
テストパターンによる欠陥のカバー率が低くなると機能不良率が高くなる。

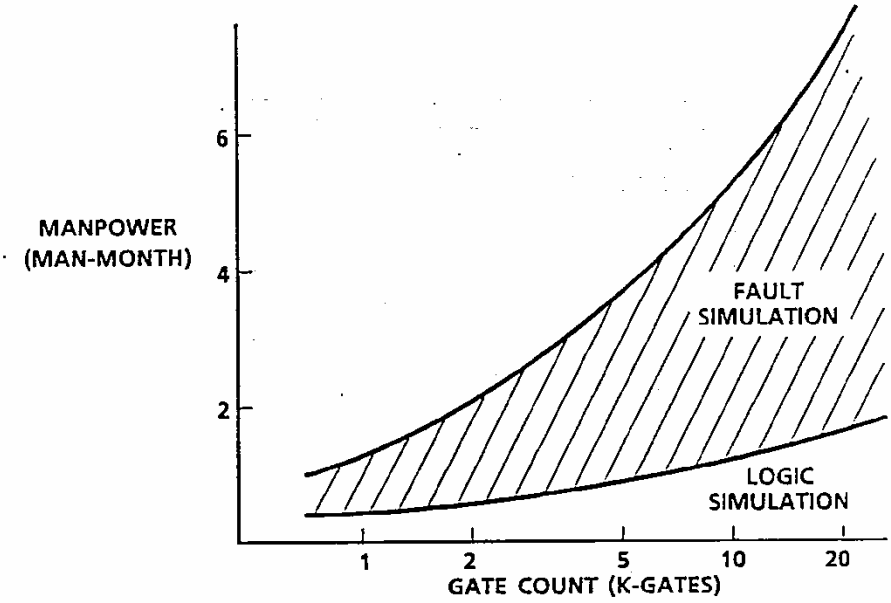

Fig. 22 MANPOWER REQUIRED FOR TEST PATTERN GENERATION

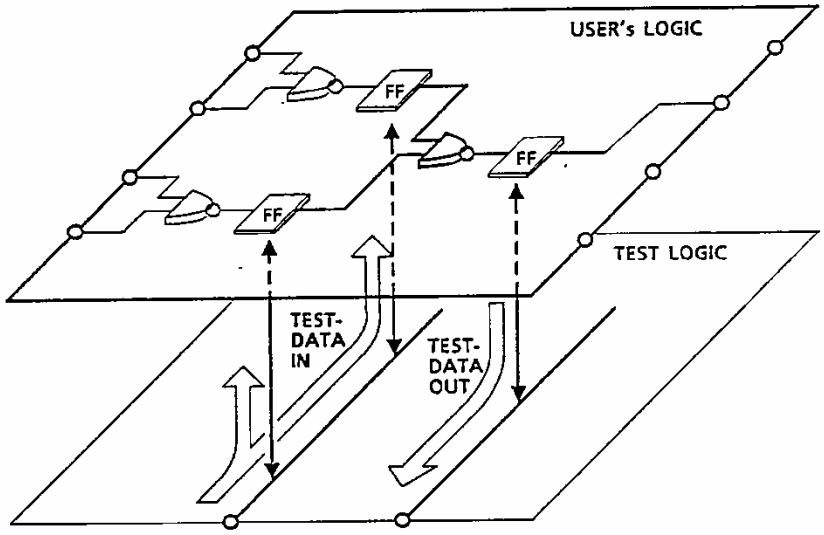

Fig. 23 AUTOMATIC TEST LOGIC ADDITION AND TEST PATTERN GENERATION

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図22 テストパターンの生成に要するマンパワー
集積ゲート数が増えると論理シミュレーション、欠陥シミュレーションの双方のマンパワーが増大するが、後者の方の増加が急激である。

図23 テストパターン生成のためのテスト回路の自動挿入
ユーザー設計の論理図のすべてのフリップフロップに対して、データの入出力を行うためのテスト回路を自動的に挿入する方式である。欠陥検出率が格段に向上する。

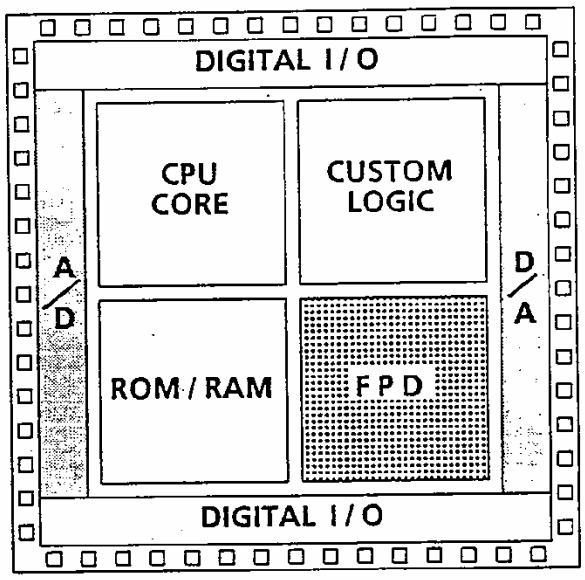

Fig. 24 FUTURE UFIC IMAGE

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図24 UFICの将来イメージ

CPU、メモリ、カスタムロジック、入出力回路を含むチップにFPD(フィールドプログラマブル・デバイス)を搭載して、ユーザー・ニーズを踏まえながらフレキシビリティーを大幅に高めることを目指している。
「解説」欄で述べたようにUFICという言葉は自然消滅となったが、図24のコンセプトは昨今のPSoC(プログラマブルSoC)の構成に似たものとなっている。