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2022
Sample shipments of 200mm SiC epi wafers begin (Resonac)
~ Process Technology ~

SiC (silicon carbide) has about three times larger band gap energy, about 10 times higher breakdown voltage, about three times faster electron saturation drift velocity, and about 10 times greater thermal conductivity in comparison with Si. It is also possible to fabricate p and n layers and grow oxide films by thermal oxidation, which are the advantage of creating MOS structures and realizing power devices with high withstand voltage and high temperature operation. Schottky barrier diodes and MOS transistors with operating voltages of several kV and handling currents of several kA have been developed and been used in bullet train cars and electric vehicles [(1)].

Currently, 4° off angle (0001) plane (c-face) 4H-SiC wafers with a diameter of 150 mm are mainly used in the industry. In order to reduce device prices, the development of 200mm diameter wafers has been awaited [(2)(3)].

Wafers are fabricated in three stages: single crystal ingot growth, slicing and polishing process, and epitaxial (epi) growth.

The sublimation (modified Lely) method has been used to produce single-crystal ingots as shown in Figure 1(a). A graphite crucible filled with powdered SiC material is heated to 2200-2400°C, and the sublimated SiC material recrystallizes on the surface of SiC seed crystal placed on the top of the crucible.

Various crystal defects (dislocations) are introduced into SiC crystals, such as micro-pipes, Threading Screw Dislocations (TSDs), Threading Edge Dislocations (TEDs), Basal Plane Dislocations (BPDs), etc. These crystalline defects cause degradation of device characteristics and therefore it is necessary to be reduced.

In 2004, Toyota Central R&D Labs and Denso invented the Repeated A-Face (RAF) method to reduce dislocations by repeated a-face growth, making full use of property that dislocations propagate mainly in the direction perpendicular to the c-axis [(4)].

An a-plane crystal is cut from an ingot grown in the c-axis direction, and is used as a seed crystal for a-plane growth as shown in Figure 2. Another a-plan crystal is cut from the grown ingot and is used as seed crystals for next a-plane growth. After this series of a-plane growth is repeated several times, c-

plane crystal is cut from the a-plane grown ingot finally, and normal c-plane growth is performed using c-plane crystal as seed crystal.

Denso, Toyota Central R&D Labs, and Showa Denko (now Resonac) confirmed that the quality of 150 mm diameter SiC wafers was significantly improved by RAF method in 2013.

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In the sublimation method, the crystal growth rate is slow (0.3 mm/h to 0.5 mm/h) and growth stops when the material in the crucible is depleted. Therefore ingot growth is limited to a length of about 30mm-50 mm. In the gas crystal growth method (High Temperature Chemical Vapor Deposition: HTCVD), as shown in Figure 1(b), the carrier gas H_2 and the source gases silane (SiH_4) and propane (C_3H_8) are introduced into a high temperature crucible. The gas temperature is raised to 2500-2550°C by induction heating, and the Si and C atoms generated by thermal decomposition of feed gas are synthesized into SiC crystals on the seed crystal surface. Continuous crystal growth is possible, and crystal growth rates of 2mm/h to 10 mm/h, about 10 times higher than the sublimation method, can be obtained. And also, it can grow crystals of two orders of magnitude higher purity than the sublimation method.

By means of developing a reactor with a small temperature distribution in the radial direction, and by optimizing the growth conditions with off-angled C-face 4H-SiC seed crystals, Denso and Central Research Institute of Electric Power Industry discovered that dislocations decreased as crystals grew in 2020. High-quality150 mm diameter SiC bulk crystals were grown with about 10 times higher growth rate than the sublimation method [(5)].

In the Top Seeded Solution Growth (TSSG) method, SiC is grown on a seed crystal from a carbon-containing Si alloy solution which is synthesized with a Si-based alloy solvent and the carbon dissolved from the carbon crucible into silicon solvent as shown in FIg.1(c). The advantage is that the temperature distribution in the crystal during crystal growth is small, making it prevent generation of dislocations. Long ingots can be grown by continuous top-seeding Si alloy. By utilizing alloy solution with high C solubility (Si-Cr, Si-Ti, Si-Nd), crystal growth rates of about 2 mm/h can be achieved.

Nagoya University has discovered that when crystals were grown on seed crystals with micro-steps several 10 nm high on the surface, threading dislocations was converted to in-plane-dislocations and stacking faults in the c-plane. By using this property, dislocations were ejected outward as the crystal grew, and high-quality SiC crystals were realized. Precise control of the alloy solution flow (thermal convection, electromagnetic convection, etc.) was necessary to maintain optimal micro-steps on the crystal surface at all times during crystal growth. Nagoya University successfully grew 150 mm diameter crystal ingots at 1860°C on 4° off seed crystals using Si-40at.%Cr-2at.%Al solution. They got high quality crystal with TSD density of 200/cm^2 by utilizing process informatics such as thermal fluid dynamics simulation. The university also has succeeded in growing 200 mm diameter crystals [(6)].

High-voltage devices require thick epitaxial layers with a thickness of 100-150 μm, which requires fast epitaxial crystal growth speed. Central Research Institute of Electric Power Industry, Denso, NuFlare Technology, and Showa Denko (now Rezonac) have developed an epitaxial crystal growth technique and equipment that achieved high-speed growth of 50 μm/h or more and uniform film thickness using a gas system containing H_2-SiH_4-C_3H_8-HCl at a growth temperature of 1550-1650°C and high-speed wafer rotation (maximum 1000 rpm) [5]. The 50th (FY2023) Iwatani Naoji Memorial Prize (for the development and application of high-speed production technology for high-quality SiC single-crystal films) was awarded for this technological development [7].

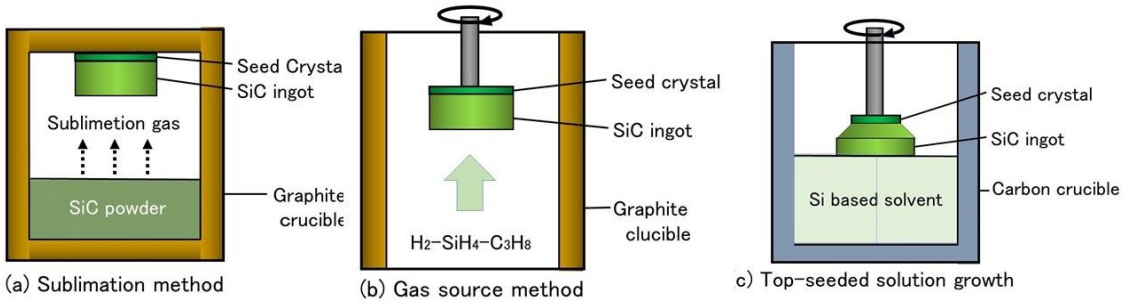

Figure 1　Schematic diagram of SiC bulk crystal growth

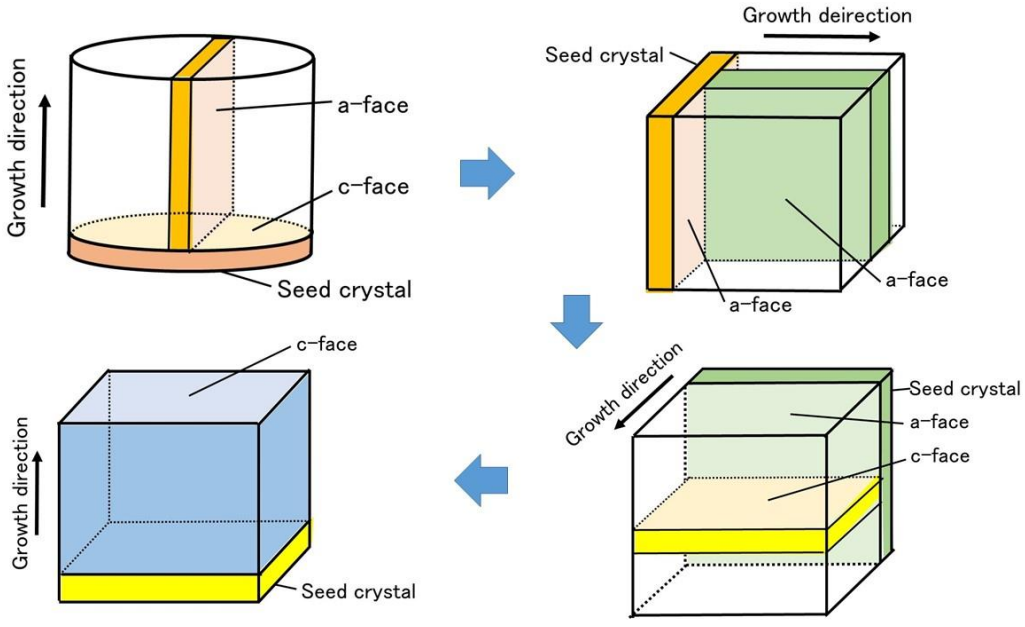

Figure 2　Process flow of RAF method
(Prepared by the Japan Semiconductor History Museum based on Reference (4))

Figure 3　SiC epitaxial wafers [2][3]
Left: 150 mm (6 inches), Right: 200 mm (8 inches)

References:

(1) Semiconductor History Museum of Japan, Discrete Semiconductor Devices, etc.,
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(3) Kenji Momose, "Development of SiC epitaxial wafers", Journal of The Japan Society for Precision Engineering, vol.88, no.12, pp. 883-884, (2022) (Japanese)

(4) Shoichi Onda, "Current Status and Future Prospects of SiC Wafer", DENSO TECHNICAL REVIEW, Vol.22 ,pp.41-50,（2017）

(5) Hidekazu Tsuchida, Isaho Kamata, Norihiro Hoshino, and Koichi Murata, "Development of crystal growth techniques for high-power SiC devices" Oyo Butsuri, vol.90, n0. 11, pp. 675-678, (2021) (Japanese)

(6) Yuki Nakanishi, Kentaro Kutsukake , Yifan Dang, Shunta Harada, Miho Tagawa, and Toru Ujihara, "Analysis of macrostep interaction via carbon diffusion field in SiC solution growth", Journal of Crystal Growth, vol. 631, 127609, (1 April 2024)

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https://criepi.denken.or.jp/press/pressrelease/2024/03_08.html