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Early 2010s
Full-scale use of FinFETs has started
~ Process Technology ~

LSIs have improved integration levels and performance by reducing the structural dimensions of planar MOSFETs. The issues associated with shortened gate lengths, such as increased subthreshold currents, generation of tunneling currents through the gate dielectric, and reduced carrier mobility due to high impurity doping, have been improved by using technologies such as strained silicon channels and high-k / metal gates [(1)(2)(3)].

However, as the design rule has decreased to 22 nm or less so that the short-channel effect has become more severe, and leakage currents have been increasingly difficult to control, alternative MOSFET structures to replace planar MOSFETs have been explored. The candidate structures were PD-SOI FETs [(5)] and FD-SOI FETs [(6)], which were developments of the XMOS Transistor [(4)] invented by Hayashi and Sekikawa (Electrotechnical Laboratory), and FinFETs [(7)] invented by Hisamoto (Hitachi) and others.

In a FinFET, the silicon substrate surface is processed into thin strips (fins) like the dorsal fin of a fish, and both sides of the fin are used as MOSFET channels as shown in Figure 1. Gate electrodes are formed across the fin. The potential of the channel region is well controlled by the gate potential, which increases the punch-through voltage between source and drain and suppresses the short-channel effect. Therefore, this enables further performance improvement through device miniaturization.

Since its proposal in 1998, FinFETs have been actively developed throughout the 2000s as a leading candidate for next generation node. In FinFETs, the fin width must be 1/2 -1/3 of the gate length, requiring even finer processing than the gate length. SideWall pattern tranfer (SWT) technique was invented to form fins of 10 nm or less in width beyond the direct resolution of ArF (192 nm) immersion lithography. Processing techniques such as Self-Aligned Double Patterning (SADP), Self- Aligned Quad Patterning (SAQP), etc., have developed using the SWT. Epitaxial growth to widen the fin width of the S/D section and metallization of the S/D region have been used to reduce parasitic resistance [(8)].

Intel commercialized FinFETs at 22 nm node in 2012 and adopted them for Core i7 and Core i5, marking the dawn of the FinFET era. Fins with a width of 8 nm and a height of 34 nm were used [(9)]. The 14nm node announced in 2014 used fins with a width of 8nm and a height of 42nm, while the 10nm node announced in 2017 used fins with a width of 7nm and a height of 46nm [(10)(11)].

(Reference: About the name)

Hisamoto et al. initially called this FET a DELTA (fully depleted lean-channel transistor), and Intel called it a Tri-Gate Transistor, but later Chenming Hu (UC Berkeley) named it a FinFET, which became the popular name.

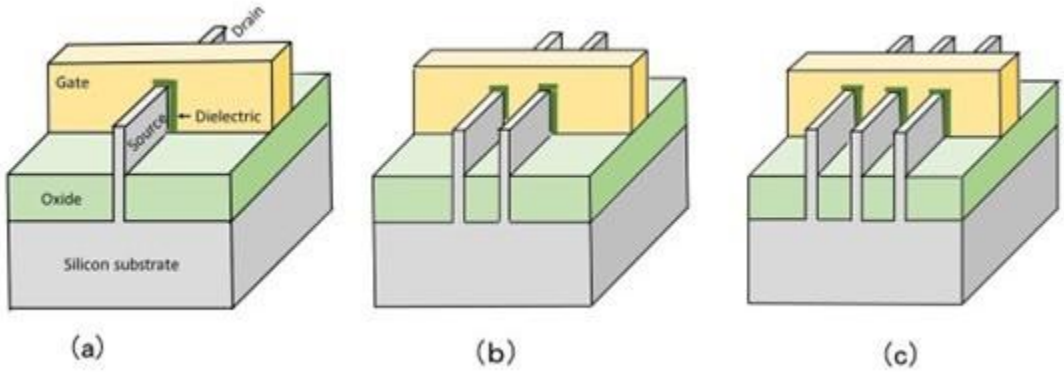

Figure 1　Schematic of FinFET Structure

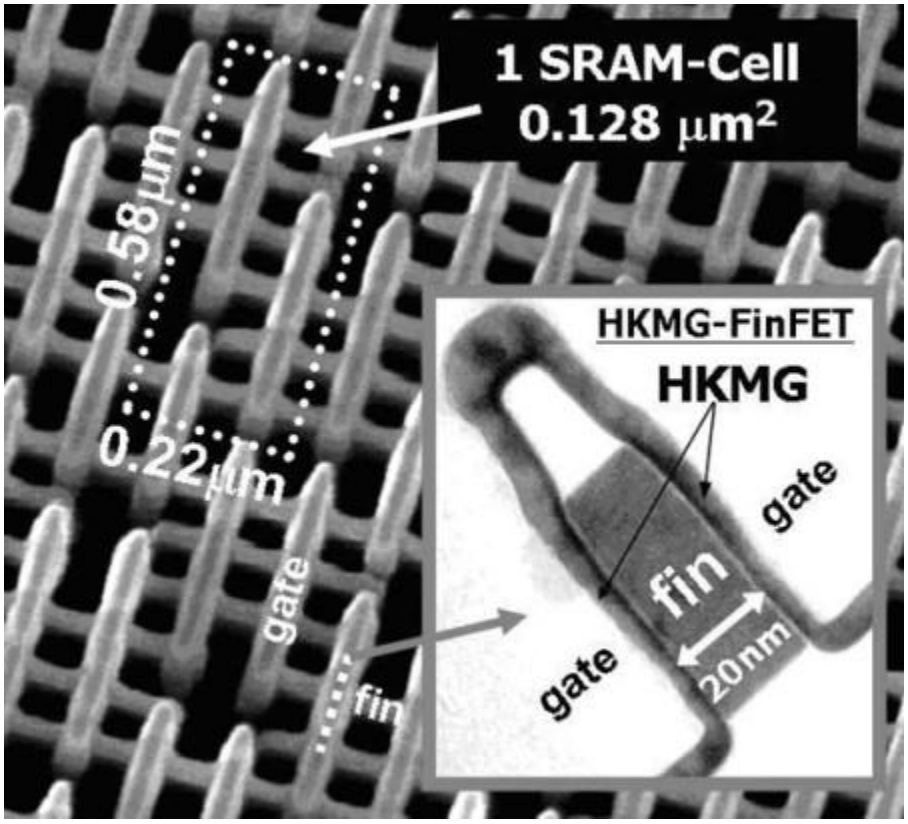

Figure 2　Cross-sectional photo of FinFET and pattern photo of SRAM using FinFET [12]
(Courtesy of Toshiba Corporation)

References:

(1) Semiconductor History Museum of Japan, Integrated Circuits, "2000s: Exploring New Structure Devices"
https://www.shmj.or.jp/english/pdf/ic/exhibi712E.pdf

(2) Semiconductor History Museum of Japan, Process Technology, "Late 2000s: Usage of strained silicon for high-speed transistors"
https://www.shmj.or.jp/english/pdf/process/exhibi416E.pdf

(3) Semiconductor History Museum of Japan, Process Technology, "Late 2000s: Adoption of high-k materials and metal gates for high-speed transistors"
https://www.shmj.or.jp/english/pdf/process/exhibi424E.pdf

(4) T. Sekigawa, and Y. Hayashi, "Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate", Solid-State Electronics, Volume 27, Issues 8–9, pp. 827-828, (1984)

(5) G.G. Shahidi, A. Ajmera, F. Assaderaghi, R.J. Bolam, E. Leobandung, W. Rausch, D. Sankus, D. Schepis, L.F. Wagner, Kun Wu, and B. Davari, "Partially-depleted SOI technology for digital logic", 1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, pp.426 - 427, (1999)

(6) M. Yoshimi, H. Hazama, M. Takahashi, S. Kambayashi, T. Wada, and H. Tango, "Two-dimensional simulation and measurement of high-performance MOSFETs made on a very thin SOI film", IEEE Trans. on Electron Devices, vol. 36, Issue 3, (1989)

(7) D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET", 1989 IEEE International Electron Devices Meeting, Digest of Technical papers, pp.833 – 836, (1989)

(8) Satoshi Inaba, "Advanced FinFET process, integration technology for 32nm node and beyond", Journal of IEICE, vol. 91, no.1, pp. 25-29, (2008) (Japanese)

(9) C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James;D. Jones;J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith. C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors", 2012 Symposium on VLSI Technology, Digest of Technical Papers, pp. 131-132, (2012)

(10) S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, T. Ghani, M. Giles, S. Govindaraju, R. Grover, W. Han, D. Hanken, E. Haralson, M. Haran, M. Heckscher, R. Heussner, P. Jain, R. James, R. Jhaveri, I. Jin, H. Kam, E. Karl, C. Kenyon, M. Liu, Y. Luo, R. Mehandru, S. Morarka, L. Neiberg, P. Packan, A. Paliwal, C. Parker, P. Patel, R. Patel, C. Pelto, L. Pipes, P. Plekhanov, M. Prince;S. Rajamani, J. Sandford, B. Sell, S. Sivakumar, P. Smith, B. Song, K. Tone, T. Troeger, J. Wiedemer, M. Yang, and K. Zhang, "A 14nm logic technology featuring 2nd-generation FinFET, air-gapped interconnects, self-aligned

double patterning and a 0.0588 μm2 SRAM cell size", 2014 IEEE International Electron Devices Meeting, Digest of Technical Papers, pp. 3.7.1 - 3.7.3, (2014)

(11) C. Auth, A. Aliyarukunju, M. Asoro, D. Bergstrom, V. Bhagwat, J. Birdsall, N. Bisnik, M. Buehler, V. Chikarmane, G. Ding, Q. Fu, H. Gomez, W. Han, D. Hanken, M. Haran, M. Hattendorf, R. Heussner, H. Hiramatsu, B. Ho, S. Jaloviar, I. Jin, S. Joshi, S. Kirby, S. Kosaraju, H. Kothari, G. Leatherman, K. Lee, J. Ieib, A. Madhavan, K. Marla, H. Meyer, T. Mule, C. Parker, S. Parthasarathy, C. Pelto, L. Pipes, I. Post, M. Prince, A. Rahman, S. Rajamani, A. Saha, J. Dacuna Santos, M. Sharma, V. Sharma, J. Shin, P. Sinha, P. Smith, M. Sprinkle, A. St. Amour, C. Staus, R. Suri, D. Towner, A. Tripathi, A. Tura, C. Ward, and A. Yeoh, " A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects", 2017 IEEE International Electron Devices Meeting, Digest of Technical Papers, pp. 29.1.1 - 29.1.4, (2017)

(12) Toshiba News, "Toshiba, IBM, and AMD Develop World’s Smallest FinFET SRAM Cell with High-k/Metal Gate", (Dec 17, 2008)
https://www.global.toshiba/ww/news/corporate/2008/12/pr1701.html

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