To search page

1987s-1980s

2-Kbit EPROM (Intel, U.S.A.)

~ Integrated Circuit ~

EPROM (Erasable Programmable Read Only Memory) performs writing by injecting electrons into a floating gate of a MOS transistor with a high voltage. Since the electrons in the floating gate are insulated from the surroundings, they are not erased even when the power is turned off, and memory function is realized. The erasing is performed by irradiating ultraviolet rays to excite electrons to pass through the insulating film of the gate. Because of the UV erase operation, EPROM is also called UV-EPROM (Ultra Violet EPROM). The package of EPROM has a window made of quartz glass that transmits ultraviolet rays, therefore package cost is high. Also, a special EPROM writer is required to write a large number of EPROMs at the same time, but EPROMs were widely used at the time because of the importance of erasable and programmable ROMs.

EPROM started in 1971 when Intel developed the world's first 2K bit EP-ROM 1702A. In the EPROM market of the 1970s, Intel and TI advanced the capacity increase as the leading makers and the Japanese manufacturers followed them. The capacity increase of the EPROM continued in the 1980s, from 64 Kbits around 1980 to a 4 Mbit product which was developed at the end of the 1980s. In the 1980s, Japanese manufacturers caught up with Intel and TI in the capacity increase trend.

Intel's 1702A was PMOS, but then NMOS also became mainstream like in DRAM. In the 1980s, shift to CMOS started, and CMOS 64K EPROM was developed by Hitachi in 1983, and other companies followed.

In order to eliminate the inconvenience of using ultraviolet rays in EPROM, the development of EEPROM (Electrically Erasable Programmable Read Only Memory) which were electrically erasable were advanced from the 1970s. Electrons accumulated in the trap levels in the floating gate or oxide film are electrically extracted using the tunnel effect. In a broad sense, batch-erase type products are also categorized as EEPROM, but EEPROM usually means byte-erase type products.

Regarding EEPROM, 16K, 64K, 256K products with cells of MNOS (Metal-Nitride-Oxide-Silicon) structure were commercialized from Hitachi.

In the nonvolatile memory market in the 1970s and the 1980s, Mask ROMs also occupied a major position. Memory capacity is easily increased in the mask ROM due to its simple cell structure, and the bit cost is low because ordinary plastic packages can be used. For this reason, in many cases, equipment manufacturers used EPROM in prototyping and debugging, and used Mask ROMs in mass production with the debugged ROM codes. Initially the mask ROM was also NMOS, but it was converted to CMOS in 1 Mbit era. In mask ROM, it was difficult to use defect repair circuit, but Hitachi developed a 16M Mask ROM equipped with a simple EPROM defect repair circuit in 1988.

Mask ROMs have the merit of low bit cost, and they were widely used in various application fields including ROM cartridges for video games. However, there is a disadvantage of long delivery lead time

and requiring a large lot size, because the writing is done in the wafer process. As a countermeasure to this, OTP (One Time Programmable) products appeared, which was a plastic molded EPROM that could be programmed only one time, and they were used for small volume applications. Since then, with the cost reduction along with the advancement of miniaturization, OTPs came to be used in medium-volume applications, too.

In the 1990s, flash memories capable of batch erase without using ultraviolet rays became widespread, becoming mainstream instead of mask ROM and EPROM.

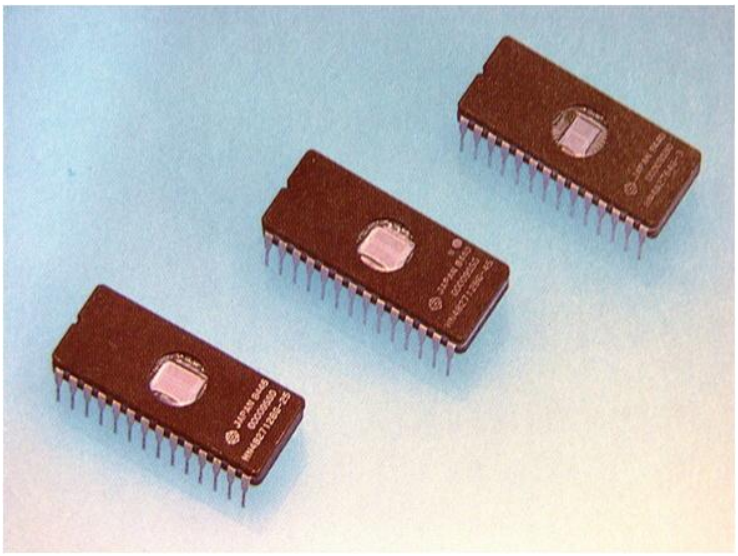

Fig.1 EPROM package with window
(By courtesy of Hitachi)

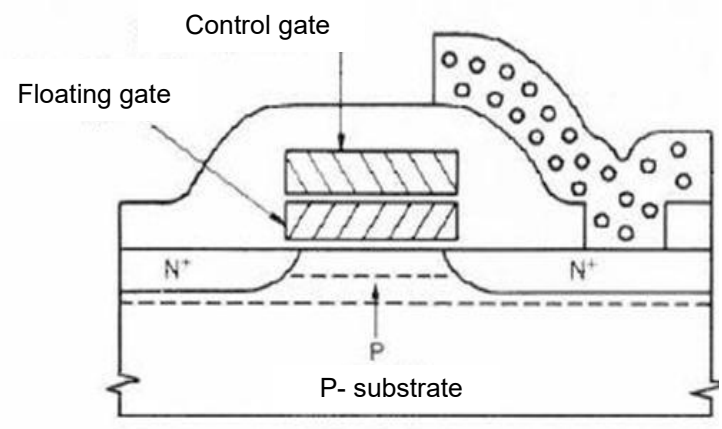

Fig.2 Memory cell of EPROM

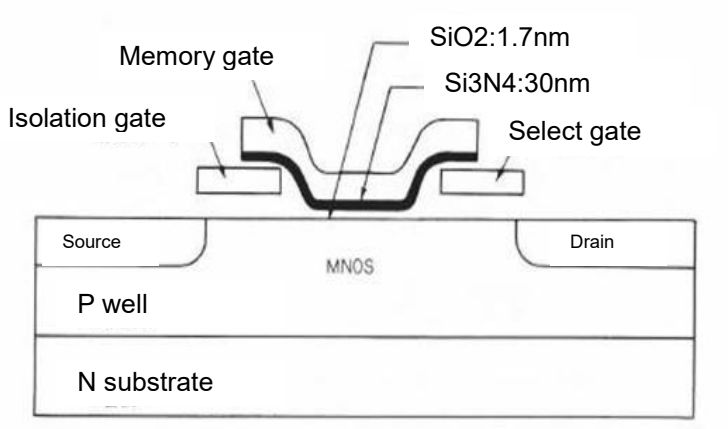

Fig.3 Memory cell of NMOS EEPROM