

1970s

Manufacturers in Japan enter the DRAM market and integration densities are improved

~ Integrated Circuit ~

The beginning of DRAM era

The dawn of DRAM era was the debut of Intel's 1K-bit DRAM 1103 in 1970. After that TI dominated the market in 4K DRAM (developed in 1973), then Mostek with 16K DRAM, and the DRAM era began which has been continuing until today. TI realized a significant reduction of chip size by changing the memory cell to the one transistor cell from the conventional three transistor cell. Mostek adopted the multi-address architecture in 4K DRAM and realized package size reduction from a 22-pin package to a 16-pin package. As a result, 1 transistor cell, multi-address, and 16-pin 300 mil wide package became the de facto standard of DRAM.

The main application field of DRAMs in this period was large-scale computers, and it was the time of conversion from conventional core memory to semiconductor memory, and the demand for DRAM greatly increased with the progress of large-scale computers.

Entry of Japanese manufacturers

Japanese semiconductor makers also entered DRAM market and actively challenged the US manufacturers in development competition. NEC developed the 1Kbit DRAM μ PD403 of NMOS in 1971, and μ PD404 in 1972. In these products, NMOS was adopted pursuing high speed, whereas Intel's 1103 was PMOS.

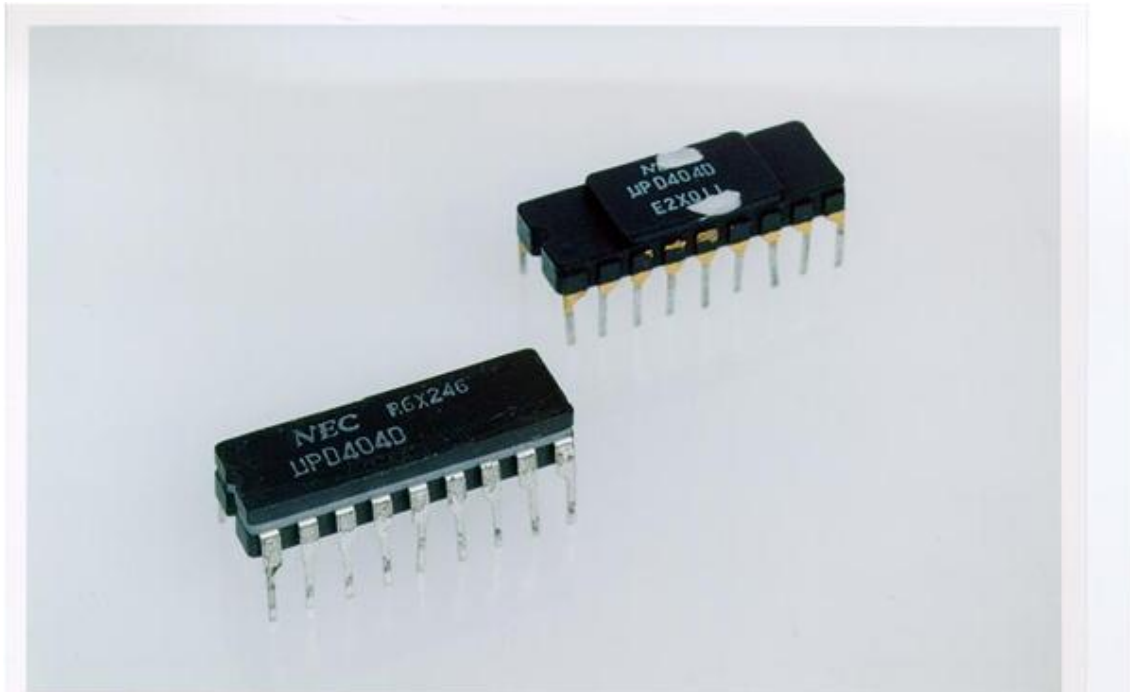
Many Japanese manufacturers started development and commercialization of 4K DRAM, but they deeply lagged to the US manufacturers on the specifications such as memory cell and multi-address architecture. In the generations of 4Kbits and 16Kbits, they could not get out of this lagging position behind the US.

Under such circumstances, the VLSI Development Project of the Nippon Telegraph and Telephone Public Corporation was started in 1975, and the VLSI Technical Research Association was established in 1976. The development of DRAM was accelerated as the frontier of microfabrication technology development.

From that time on, excellent technologies such as double-intersection bit cell architecture of DRAM memory (invented by Kiyoo Ito of Hitachi in 1974) that minimized the noise to the stored signal were devised and Japanese technology gradually began to precede the United States also in a single 5-volt architecture. In the 64K DRAM generation, Japanese manufacturers actively pursued development and gained the top market share in the global market, taking the lead to the US. At that time, a soft error

problem (SER) occurred which caused unexplained random failures in the memory operation, and it became clear that the cause was destruction of stored data by α -ray, and countermeasure were taken by the improvement of memory cell structure and increase of storage capacity.

Japanese-made DRAMs won high evaluations of reliability from computer manufacturers in Japan and the US and they steadily accumulated their skills.



μ PD 404D, 1024-bit N-channel MOSRAM