To search page

1984

Flash memory released (Toshiba)

~ Integrated Circuit ~

The first announcement of flash memory which have grown to representative nonvolatile memory was made at IEDM in December 1984 by Fujio Masuoka who worked at Toshiba at that time. The memory cell was a NOR type using three-layer polycrystalline silicon, and it was characterized in that the memory could be electrically erased collectively. Masuoka later announced the NAND type flash which could further increase the integration in 1988. NAND type flash has evolved to large capacity memory which created large demand centering on imaging applications, and has grown into a large field that drives memory technology replacing DRAM position. The naming of Flash by Masuoka et. al came from its ability of erasure all at once like a camera's flash, and this name has been established as a product name along with the subsequent growth of the market.

There were various problems in the nonvolatile memory before the flash appeared. FAMOS (Floating Gate Avalanche Injection Metal Oxide Semiconductor) developed by Intel in 1971 was a method of accumulating charges in the floating gate by avalanche injection, and ultraviolet rays had to be irradiated for 20 to 30 minutes, and a special package having a window structure transmitting ultraviolet rays was necessary. An EEPROM that was electrically erasable was announced by Yasuo Tarui et al. In 1971, but there was still a problem in reliability. Intel solved this problem of EEPROM and put it into practical use as FLOTOX (Floating Gate Tunneling Oxide) in 1980. However, FLOTOX required transistors for cell selection in order to perform writing/erasing on a bit-by-bit basis, and since one bit was composed of two transistors, the degree of integration could not be increased.

Masuoka then adopted a method of removing the cell selection transistor, increasing the degree of integration, and erasing the memory all at once as announced in 1984 (Fig.1). The memory is written by tunnel current by the FN (Fowler-Nordheim) mechanism from the channel, written in the floating gate, and erased collectively by the erase gate. Along with other control gates and floating gates, it was fabricated by three layers of polycrystalline silicon technology. The batch erasing method was consistent with the requirement for large capacity recording such as subsequent image and sound applications.

Figure 2 shows the structure and circuit configuration of a NAND type cell that Masuoka announced at IEDM in 1988. Unlike NOR type, cell transistors were connected in series except for the contact holes. As a result, the degree of integration of NAND flash dramatically increased, and finally 1G bit density was realized prior to DRAM. In addition, a multilevel cell (MLC (Multi Level Cell)) technique in which memory writing is performed at multiple levels, and assembly technology in which the chips are thinned and stacked advanced, and the capacity has been increased and the cost per bit has been decreased. The NAND type is suitable for data storage in which its large capacity is effective, and is widely used in digital cameras, audio, mobile phones, and the like. On the other hand, since the NOR type has a

high-speed random access capability, despite its difficulty in integration, it is used, replacing the conventional ROM, as a system memory for microprocessors. Both NOR type and The NAND type made progress in separate fields. The combined worldwide flash memory market is over 26 billion dollars in 2010, and is expected to show a yearly growth rate of more than 10% over the next five years.

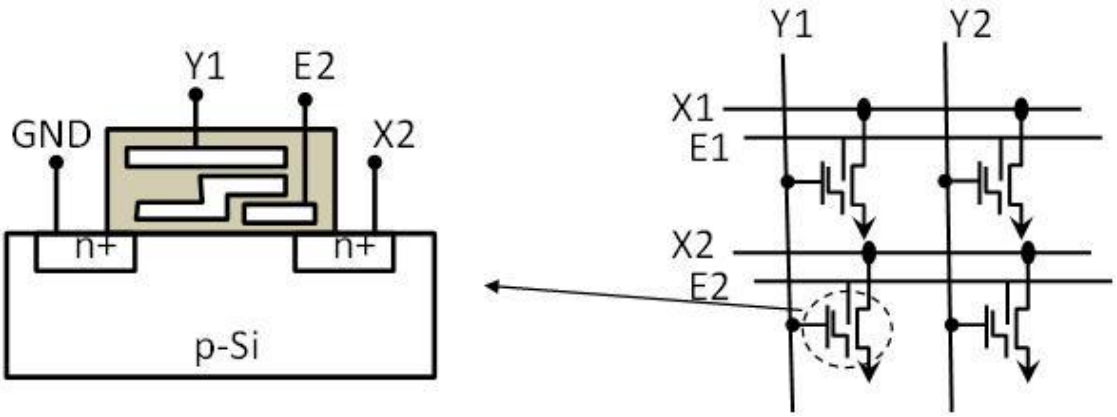

Fig.1 Memory cell structure (left) and circuit diagram (right) of Flash EEPROM

Version 2019/1/23