To search page

Early 1980s

Gate-array and standard-cell ASICs are released and evolve

~ Integrated Circuit ~

In the 1980s, as applications of digital LSIs expanded, it became difficult for conventional general-purpose LSIs to deal with these applications, and custom design of LSIs to meet the requirement of each application became necessary. These custom-designed logic LSIs are called ASICs (Application Specific ICs), and their growth was expected. The method of starting the design from the transistor level is called a full custom ASIC, in which the degree of freedom of design is high and the operation of the LSI is high, but it requires a lot of human resources with high cost. Most ASICs were products of so-called small quantities and many kinds, so how to efficiently develop and manufacture products at low cost became a big problem.

Gate arrays appeared in this situation. In the gate array, LSI called "master slice" with spread array of basic gates, such as AND and OR, is made up to the middle process, waiting for the designation by the user. Metal interconnects are defined according to the required logic function. As a result, the development period could be significantly shortened and the development cost could be reduced.
LSI Logic (LSI Logic Corporation) launched the business of the gate array for the first time. It designed and manufactured custom gate arrays using its own CAD tool called Logic Design System (LDS). Following LSI Logic, Japanese manufacturers entered the gate array business, actively expanded their business by utilizing miniaturization technology, and dominated the market. At that time, speaking of ASIC, it meant gate array. On the other hand, however, the gate array tended to waste the chip area, resulting in limitation of the degree of integration, and there was a limitation in performance since usable gates are limited to basic ones only.

On the other hand, in the standard cell system, macro-cells optimized for device dimensions from a transistor level, such as RAM and ROM, CPU, analog circuits, etc., are prepared, and their arrangement and wiring are freely specified. Since the manufacturing of the LSI can be started at the time when the placement of the macro-cell is completed, the development period from the completion of the logic design is almost equal to that of the gate array and a high-performance LSI can be realized. Compared to the full custom method, the degree of freedom in design is low, but it is more flexible than the method in which the gate arrangement is fixed like a gate array, and the design is easy. Each cell has an excellent degree of integration because its dimensions are optimized.
Although VLSI Technology led the initial business of the standard cell system, Japanese manufacturers also entered one after another. Note that the standard cell is sometimes referred to as a cell base IC by some makers.

Embedded cell arrays are positioned between the gate array and the standard cell. In this method, a desired macro cells are embedded in the base of the gate array. Since the fabrication can be started by determining the gate array and the embedded macro cells, a high-performance LSI can be realized in a short period as in the gate array. However, the performance in the gate array part is limited, and the point that a useless region easily occurs is similar as the gate array.

Gate arrays have been used for LSIs of small quantities and many kinds, but today, more flexible FPGAs (Field Programmable Gate Array) are taking over the market. Moreover, the full custom method is used only for some high-performance CPU etc. due to the difficulty of design. In this regard, the standard cell has advantages of both sides of flexibility and high functionality, and is the most widely used method in today's ASIC. Various digital/analog IP cores can be mounted, the degree of freedom of terminal arrangement is high, and clock control of the internal circuit is also possible. In the latter half of the 1990s, memories such as DRAM, Flash and so on came to be integrated. It is also used for SoC (System-on-a-chip) design.

Version 2019/1/23