To search page

1980s

EDA tools for ASIC appear

~ Integrated Circuit ~

In 1980 LSI Logic Corporation developed the industry's first ASIC product line and designed and manufactured custom gate arrays using LDS (Logic Design System), a proprietary CAD tool. Although the first product was based on high-speed ECL technology, it soon shifted to CMOS which realized low price and low power consumption. LSI logic gradually increased product lineup and IP libraries, and added standard cells, structured arrays, DSPs, and microprocessors (MIPS and SPARC). LDS was a group of design tools described in FORTRAN which input Boolean expressions and component diagrams and converts them into logical diagrams, parts lists, board layouts, routing lists, and diagnostic data. LDS was also provided outside the company and was applied to the design works outside the company, at the design centers and at the customer sites.

Likewise, VLSI Technology is a company that led the ASIC business with the standard cell system (cell-based technology). VLSI Technology's design tools included not only logic diagram input and logic simulation but also cell-based automatic place and router (chip compiler), data path compiler, RAM/ROM compiler, and state machine compiler. These design tools were integrated as a complete tool system for LSI designs, not as individual tools.

The designer edits transistor level circuit diagrams and logic diagrams, executes DRC and LVS by executing automatic placement and routing, extracts actual wiring capacitance etc. from the layout result and calculates SPICE (Simulation Program with Integrated Circuit Emphasis) execution of simulation and placement in logic diagram database, and can verify back-annotated timing information and gate size change after wiring. The characterization tool for cell library creation was able to automatically generate not only library data to be used with tools, but also data sheets for customers to use in conjunction with FrameMaker.

VLSI Technology's implementation design tool was important not only for the ASIC business but also for establishing the commercial EDA industry. Until VLSI Technology and LSI Logic, a major ASIC competitor, establish the ASIC industry, there was no commercially available tool which supported implementation designs of hundreds and thousands of ASIC products, without depending on the skilled layout technicians.

From this time, EDA vendors developing automatic layout tools began to appear.

As layout CAD, 1985 Tangent Systems Corporation announced Tangate, the automatic placement and routing for gate arrays, and Tancell, the automatic placement and routing for standard cells, and it began to spread. A library description format LEF (Library Exchange Format) and a design information description format DEF (Design Exchange Format), which are the de facto standards of the layout CAD, were created. In 1989, Tangent Systems was acquired by Cadence Design Systems (founded in 1988).

In 1991, VLSI Technology spun off the EDA division and library division to establish Compass Design Automation, and in 1997 Compass Design Automation was acquired by Avant!
Later GateEnsemble from Cadence Design Systems and GARDS from Silvar-Lisco for gate array automatic placement and routing, and Cell3 Ensemble from Cadence Design Systems, Apollo from Avant! etc., for standard cell automatic placement and routing appeared. They originally targeted at semi-custom products such as gate arrays and standard cells, and they evolved to more versatile products. In the layout CAD tool, since it was necessary to process a large number of graphic data at high speed, the research results of computational geometry were also utilized to improve the performance, and the development of the commercial EDA industry started. Along with this, the development resources of in-house EDA tools of semiconductor companies gradually shifted to the state-of-the-art technology field.

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