To search page

Late 1980s

HDLs and logic synthesis tool released

~ Integrated Circuit ~

In the early 1980s, it was becoming difficult to cope with the increase of design scale, complicated logic, and miniaturizing manufacturing processes by the traditional design method based on logic diagrams. In order to cope with this situation, various kinds of HDL (Hardware Description Language) were proposed which were easy to describe the parallel operations of hardware with truth table, state transition description and logical expression not depending on a specific manufacturing process.
In 1985 Automated Integrated Design Systems (later renamed Gateway Design Automation, and acquired by Cadence in 1989) developed Verilog HDL which is HDL and Verilog-XL logic simulator.

On the other hand, in 1987, the Department of Defense developed the VHDL (Very High Speed Integrated Circuit Hardware Description Language) that descended from Ada, in order to clarify the design specifications of ASIC products used in the delivered equipment. That is, it is the beginning that aimed at substitution of paper manuals which tended to be thick and complicated.
With these HDL and HDL simulators, LSI designers could design at more abstracted level than logic diagram which was based upon manufacturing process dependent cells. And feasible scale of design complexity was dramatically increased.

In HDL, hardware is described at abstraction level, namely register transfer level (RTL). At this abstraction level, hardware is described by using arithmetic units, registers and signal transmissions between them. Also, in many HDL's, it is possible to design a circuit by dividing it into partial circuits in nesting structure. Alternatively, existing circuit description can be reused as a partial circuit. Efficiency of design is improved by this reuse.

Initially many HDLs appeared disorderly, but IEEE standardized VHDL and Verilog HDL. And other HDLs became less used. However, VHDL and Verilog HDL have common weak points. Both of them are weak in simulation of analog circuits and mixed circuits of analog and digital, and they cannot describe a recursive logical structure. Therefore, some HDLs that overcame these weaknesses of VHDL and Verilog HDL appeared, but they have not replaced VHDL and Verilog HDL.

In the late 1980s, a logic synthesis tool which used HDL appeared, and HDL became prominent in digital design community.　In 1988, Synopsys announced Design Compiler, which became a synonym for logic synthesis later. The logic synthesis tool compiles the source file described by HDL register transfer level (RTL), and generates netlist description of manufacturable logic gates and flip-flops. In the initial systems, skills were required to write synthesizable RTL description and design constraints.

The netlist synthesized from RTL tended to be larger in size and lower in performance compared with conventional manual design. Thus, the logic synthesis tool itself needed improvements. In addition, requirements for design scale increase and shorter design time as well as shortage of design engineers were the issues. In 1990, static timing analysis technology and equivalence verification technology were established, and then the logic synthesis tools finally became commonly used.

Besides, a series of automated inspections are performed, prior to logic synthesis, on the HDL description. In this inspection process, it is possible not only to check simple descriptive style, but also to find out where it is likely to cause problems with RTL simulation, logic synthesis or automatic layout, which are the design process of the latter stage. Also, by unifying the naming rules and description formats, the readability of the HDL description and the reusability can be improved.

Version　2019/1/23