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1980s

SRAM capacities increase

~ Integrated Circuit ~

In the 1980s, 16K (2K × 8) SRAM became widely used, and further development of 64K (8K × 8) advanced. These are the products of the category called medium speed SRAM. In the 64K generation, there were two types of SRAM, a pure CMOS type product using a 6-transistor CMOS memory cell composed of PMOS and NMOS, and a CMOS peripheral type, in which the memory cell was composed of 4 NMOS and 2 high resistance loads. In the complete CMOS type, the power consumption during standby was extremely small, but the cell size was larger and the chip cost was higher. In the era of medium speed 64K SRAM, most US manufacturers withdrew from this market, and Japanese manufacturers got unrivaled position in this field. Among Japanese manufacturers, Hitachi and Toshiba took the lead in this market.

A 2μm process was adopted for 64 KSRAM, and the miniaturization advanced further, and in 256 K generation, 1.2 - 1.3μm process was adopted. 256K (32K × 8) SRAM was announced by Toshiba at ISSCC in 1984, and subsequently Hitachi, NEC and Mitsubishi at ISSCC in 1985. New technological challenges emerged as miniaturization progressed from this time. For example, the problem of soft error became evident from the 16K generation. In addition, suppression of the short channel effect of the MOS transistor and hot electron countermeasure also became important as the miniaturization advanced. As a countermeasure against lower yield, defect relief was introduced from around 256 KSRAM.

Medium speed SRAMs of 1Mbit (128k x 8) were released in 1988, in which Hitachi and Toshiba took the lead. 0.8μm process was used. Furthermore, from 1989 to 1990, the development of 4 Mbit SRAM was announced from various companies at ISSCC, product shipping started, and SRAM capacity increase progressed.

Although the SRAM capacity increase progressed steadily, the SRAM market gradually shifted to DRAM since the late 1980s. To begin with, the cost per bit was disadvantageous in that SRAM bit cost was four times that of DRAM, but SRAM was superior to DRAM in terms of ease of use in small systems. However, usability of DRAM was improved by the implementation of auto-refreshing function which eliminated troublesome refreshing operation, and by the implementation of refresh support function on MCU, and further by the appearance of x4 configured DRAM, and DRAM started to be used also for small systems. In addition, the decrease in application dedicated equipment due to the spread of personal computers also reduced SRAM market growth.

For this reason, a product called pseudo SRAM emerges. Pseudo SRAM was based upon CMOS DRAM technology, yet pin compatible with SRAM, which was convenient for small systems. Since DRAM memory cell was used, cost per bit was lower than SRAM. Pseudo SRAM appeared in the 1970s in the United States, and Japanese manufacturers, Hitachi and Toshiba, commercialized it from 256K.

Pseudo SRAMs were commercialized up to 4 Mbit. Along with the increase in capacity, miniaturization of SRAM packages also progressed. A surface mount type SOP (Small Outline Package) was introduced in place of the conventional DIP (Dual Inline Package), and a thinner TSOP (Thin Small Outline Package) appeared.

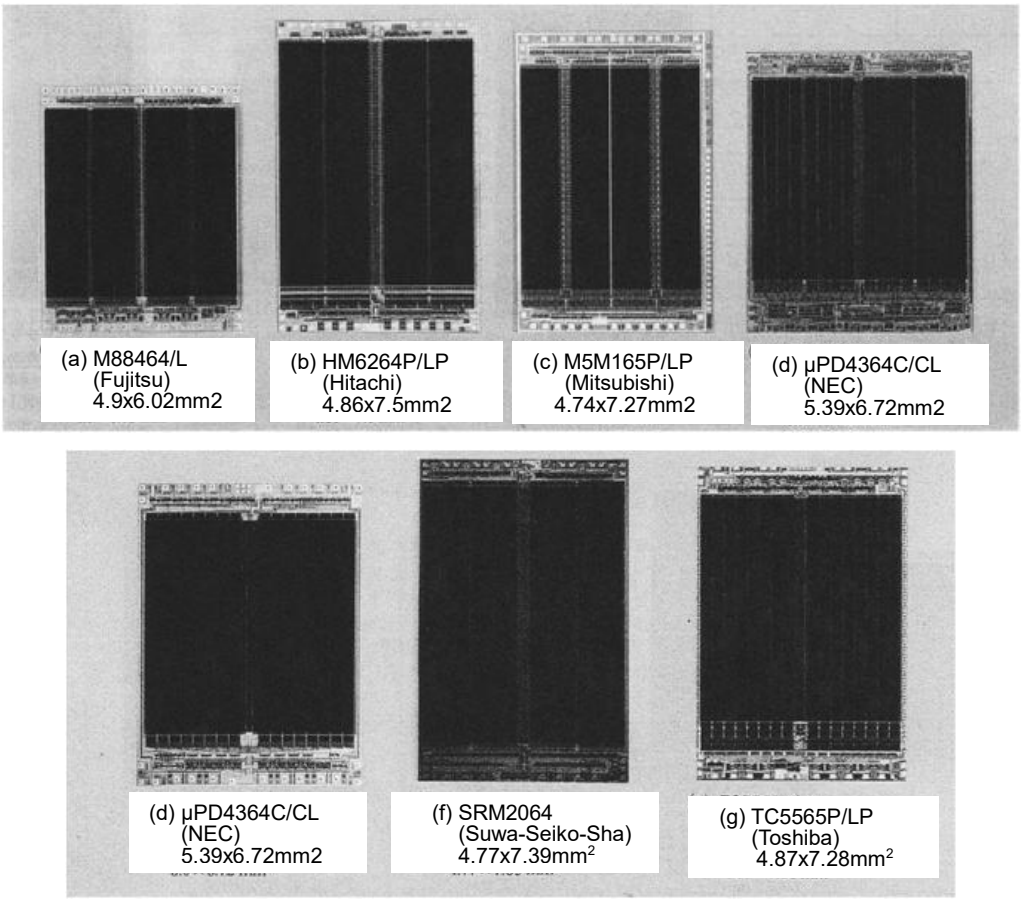

Fig 1: CMOS peripheral type 8kx8 SRAM

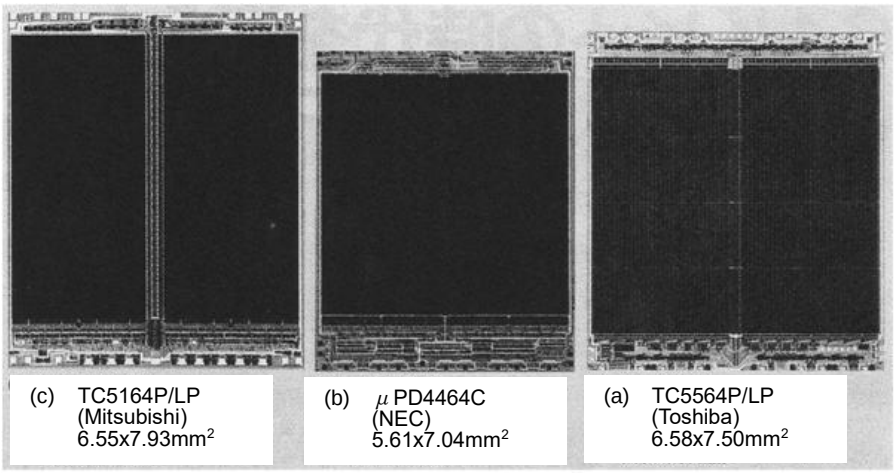

Fig.2: Pure CMOS type 8kx8 SRAM

Version 2019/1/23