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1980s

Advanced CAD tools and the shift to the EWS

~ Integrated Circuit ~

Since around 1980, semiconductor companies developed and used their in-house EDA tools operating on mainframe computers for the LSI design support, such as logic circuit diagram input, logic simulator, timing verification, fault simulator, layout CAD (floor planner, automatic placement and wiring), layout verification, mask generation, etc.

Meanwhile, specialized tool vendors such as Mentor Graphics, Daisy and Valid Logic appeared which offered CAE (Computer Aided Engineering) systems for logic circuit design of customized products.

There were platforms using general-purpose EWS made by Apollo Computer (Mentor Graphics) and those using dedicated hardware and OS (Daisy, Valid Logic). And then WS (Work Station) from Sun Microsystems became popularized, and Linux-based general purpose EWS (Engineering Work Station) became commonly used. These tools were a combination of a graphic editor for inputting a logic circuit diagram and a logic simulator for verifying the operation thereof. A fault simulator for detecting a single degenerated fault of a logic circuit, a timing simulator for timing verification, and the like were put to practical use.

In addition, with the spread of EWS, the design environment such that each designer occupies EWS and design tools has become a common practice.

As layout CAD, Tangate and Tancell provided by Tangent Systems started to spread in 1985. A library description format LEF (Library Exchange Format) and a design information description format DEF (Design Exchange Format), which is the de facto standard of the layout CAD, were created.

In 1983, ECAD's (later acquired by Cadence) Dracula appeared, which had Design Rule Checking (DRC) and Electrical Rule Checker (ERC) of layout data created by layout CAD, and Layout Versus Schematic (LVS) function to compare layout data and logical data. In addition, back annotation technology was developed, in which parasitic elements (capacitors, resistors, inductors, etc.) in the created layout data were extracted, the information was added to the original circuit, and circuit and logic simulation was performed again, thereby the correct function of the laid-out circuit satisfying the target performance was assured, and circuit and logic verification in the form close to the real system became possible before completing the mask data.

As a result of multiple vendors offering various tools, problems such as incompatibility of design data among the tools arose. Cadence and Mentor Graphics, two major vendors at the time, made moves to incorporate other companies' products into their frameworks called “Framework”, respectively, but they were not successful. For this reason, research on EDIF (Electronic Design Interchange Format) as a common format for exchanging design data started in 1983, and the results were published as EDIF100 in 1985, EDIF200 in 1988, EDIF300 in 1993, and final version EDIF400 in 1996.

Fig. EWS Dn330 from Apollo Computer

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