To search page

2014

Development of 3.3 kV/1.5 kA SiC-MOSFET (Mitsubishi)

~ Discrete Semiconductor/Others ~

Since the band gap of SiC is as large as 3.25 eV, withstand voltage of dielectric breakdown is about 10 times larger than that of Si, and since it has high intrinsic temperature, it plays as a semiconductor even at high temperatures. From these properties SiC is suitable semiconductors for power devices handling high voltage and large current. The merit of high dielectric breakdown voltage is remarkable in kilovolt-class power devices. Even in 3.3kV withstand voltage region where Si cannot be used because of too high ON-resistance, MOSFET can be made using SiC. By using SiC, a switching device with 3.3 kV withstand voltage was realized with low losses both in conduction and in switching which are two main loss factors in power devices.

Bulk crystal growth by sublimation method at higher than 2,000°C is required for SiC wafer fabrication. Due to technical difficulties, fabrication of SiC wafers were delayed compared to Si, but in the latter half of the 1990s, wafers of 2” diameter became available, and device development became active. With regards to the quality of SiC wafers, device killer defects such as large screw dislocations which were initially big problems were reduced, and defects in the epitaxial growth layer are being steadily reduced.

Figure 1 shows the cross-sectional structure of the MOS cell of a 3.3 kV SiC-MOSFET. It is a vertical planar MOSFET that conducts current from the drain electrode on the back surface to the source electrode on the surface. A high voltage was held by a p-n junction formed between the p-type well region and the n-type drift layer. For the substrate, a 4H-SiC polytype Silicon Carbide suitable for a power device was used and an n-type drift layer was epitaxially grown. Resistance reduction of the junction transistor region (JFET region) is effective for reducing the resistance of the high-voltage SiC-MOSFET, and the width and doping concentration of the JFET region were optimally designed. Compared with Si, more electron trapping levels exists at the MOS interface of SiC, which hinders resistance reduction of MOS channel. The influence of the electron trap level was reduced by optimizing the doping profile design of the MOS channel part and the high temperature heat treatment of the gate oxide film, realizing low resistance of the MOS channel and stabilization of the threshold voltage.

Mitsubishi Electric successfully developed a 3.3kV/1.5kA full SiC power module equipped with 3.3kV SiC-MOSFET and SiC-SBD. It commercialized an inverter for railway cars (Fig.2) equipped with 3.3kV/1.5kA full SiC power module in 2014 and demonstrated significant energy saving effect in commercial operation in 2015.

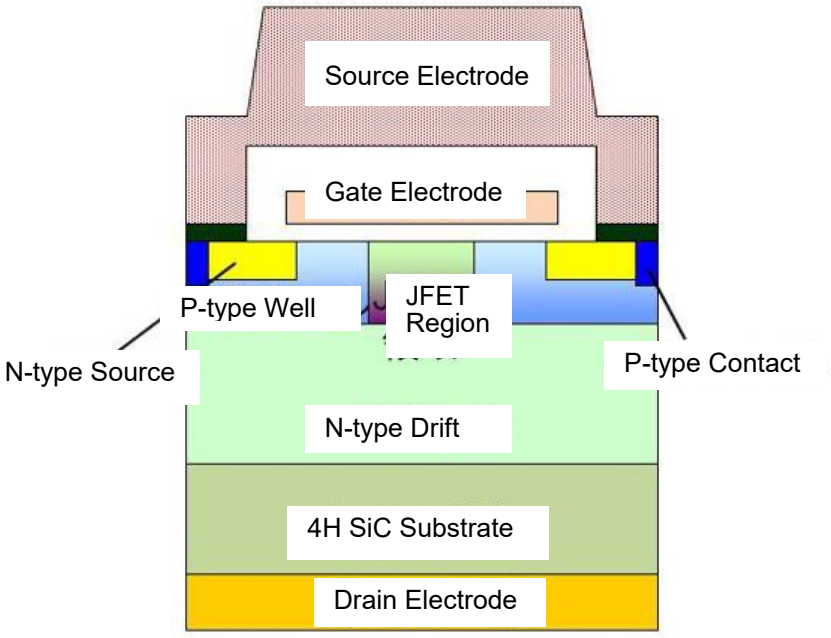

Fig. 1: Cross-sectional structure of MOS cell part of 3.3 kV SiC-MOSFET

Fig. 2: Inverter for railway car applied with 3.3kV/1.5kA Full SiC Power Module
(By courtesy of Mitsubishi Electric)

References:

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