To search page

1975-85
Improvement of photodiode for image sensor (Sony, Hitachi, NEC, Toshiba)

~ Discrete Semiconductor/Others ~

Photodiodes are used for photodetectors of image sensors. In 1987, Sony developed a 2 / 3-inch, 380,000-pixel CCD image sensor using a new type of photodetector, now called a Pinned Photodiode (Sony named it HAD: Hole Accumulation Diode) [1], and installed it in the 8mm VTR integrated video camera "CCD-V90". In the 1990s, the era of passport size video cameras demands compact CCD image sensors with large numbers of pixels (1/2 inch or smaller with 400,000 pixels or more). As a result, Pinned Photodiodes came to be widely used in CCD image sensors by manufacturers [2]. In 1995, Kodak adopted them for CMOS image sensors. Pinned Photodiodes became the primary photodetector for CCD / CMOS image sensors. The Pinned Photodiode (also known as Buried Photodiode) technology was established as a widely used standard technology by active proposals of photodiode improvements from the late 1970s to the early 1980s.

The Pinned Photodiode is a photodiode in which the entire N layer is covered with a P layer. The part of the P layer on the light incident surface is heavily doped P^+(Fig.1). Kodak named this structure Pinned Photodiode in 1984 because the P^+ surface of the light incident surface was pinned to the substrate potential. This device has features such as high light sensitivity, wide dynamic range, image lag free, much smaller dark current due to reduced influence of GR center on the light receiving surface, and no white scars.

In 1975, Sony proposed using a PNP transistor as the photodetector [3]. By providing a P^+ layer (emitter) for the light incident section, the sensor electrode that covers the entire light receiving surface of the photodiode can be eliminated to improve the light sensitivity greatly. It was a basic proposal for a pinned photodiode with a P^+ layer on the surface of the light receiving part.

Next, proposals were made separately by Hitachi and Sony to use the P^+ layer as the substrate potential. In 1977, Hitachi presented a structure in which the high-concentration surface P^+ layer is connected to a P-type substrate (well) and pinned it to the same potential as the substrate to increase the charge storage capacity and widen the dynamic range of the photodiode [4]. In 1978, Sony announced an FT (Frame Transfer) -CCD image sensor, using the photodiode with the same structure [5]. Sony succeeded for the first time in the world in prototyping a VTR-integrated color movie camera using a 2 / 3-inch 280,000-pixel FT-CCD image sensor that developed this technology, in 1981 [6].

In 1977, Toshiba proposed optimizing the impurity concentration and thickness of the charge storage N layer of the PN junction photodiode to completely deplete it in order to reduce image lag and improve light sensitivity [7]. In 1980, NEC analyzed in detail the relationship between the electric potential of the N layer of a photodiode in which the P layer was pinned to the substrate potential and the potential of the transfer gate to an external circuit. They then demonstrated a principle of operation that completely transfers the signal charges while keeping the potential of the depleted N layer higher than the channel potential of the transfer gate by a required value or higher, realizing image lag free operation [8][9]. The design methods based on this operation principle of the pinned photodiode focusing on this N-layer potential were widely studied and have been standardized as the Pinned Photodiode for today's CCD and CMOS image sensors.

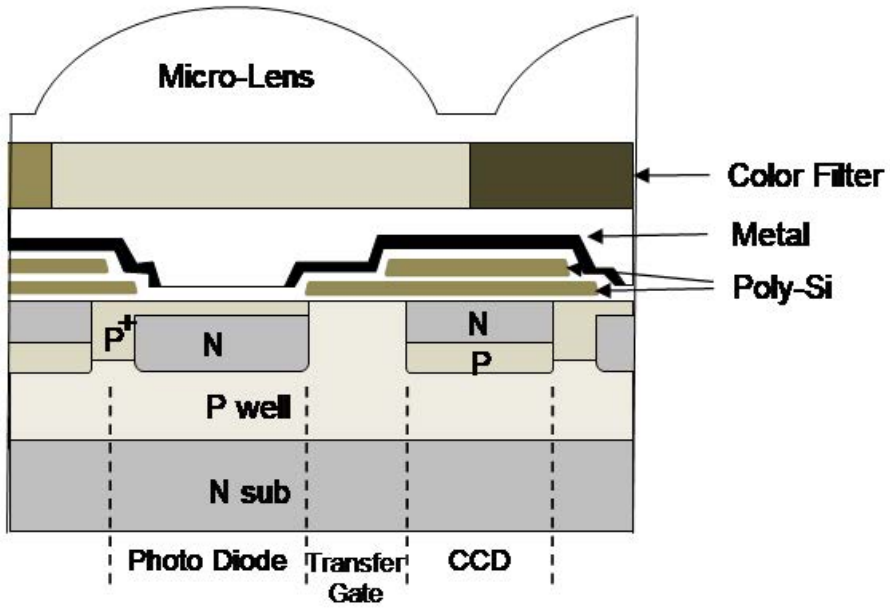

Fig-1 Cross-sectional structure of the IT-CCD image sensor (surface irradiation type)

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