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Development of a pixel/DRAM/logic 3-layer stacked CMOS Image Sensor (Sony)

~ Discrete Semiconductor/Others ~

The development of a two-layer stacked CMOS Image Sensor (CIS), in which pixels and logic were stacked, had enabled improvements in imaging characteristics and the incorporation of new functions of CISs for mobile applications [(1)(2)]. The pixel and logic wafers were fabricated separately and bonded together, allowing processes to be optimized for each wafer. This not only improved image quality, but also enabled the use of advanced logic, which in turn enabled the incorporation of advanced circuits such as high dynamic range (HDR) video and image plane phase-difference detection AF processing functions. The stacked CIS was made possible by the development of technology for high-precision bonding of the pixel wafer and the logic wafer, and Through-Silicon Via (TSV) technology for electrical connection.

However, in the conventional CIS, signals from pixels were processed by a logic circuit and read out sequentially from the I/F (Fig. 1(a)), so the readout speed of the CIS was limited by the speed of the I/F and could not be increased. As a result, as an example, the readout speed of all pixels could only be increased to 30 fps, and rolling shutter distortion occurred due to the time difference between the first and last pixels read out, as shown in Figure 1(b). As shown in Fig. 1(c), the readout speed could be increased avoiding the speed limits of the I/F by installing a DRAM that temporarily stored the signals from the pixels. As a result, a CIS with 120 fps readout was able to develop and rolling shutter distortion was reduced. (Fig. 1(d)) [(3)(4)]

The key points of this 3-layer stacked CIS development were as follows.
(1) Development of technology to bond three wafers of pixel/DRAM/logic (Fig. 2)
A manufacturing method was established for stacked chips without sacrifice mass production.

(2) Development of technology that enables thinning of DRAM Si substrates to approximately 3 μm thick while maintaining their characteristics.
The same chip size and thickness as the 2-layer product was achieved in spite of the 3-layer laminate.

(3) Development of a 2-layer TSV for electrical connections between wafers to achieve low resistance and low parasitic capacitance (Fig. 3)
Wide bandwidth and low power communication between DRAM and logic was achieved

The above technology enabled high-speed readout from the pixel, resulting in images with minimal rolling shutter distortion (Fig. 1(d)). In addition, a super slow movie was realized as follows. If the sensor detected a user's trigger or rapid motion in a scene while taking a movie in full HD at 30 fps, then the readout speed would change to 960 fps. The data for this high-speed movie was stored once in the DRAM and then the sensor changed the speed back to 30 fps. The data stored in the DRAM was sent out of the sensor in the I/F spare time using MIPI's virtual channel. The movie picture was reconstructed by inserting the data between the 30 fps video flams. (Fig. 4 [5]).

This device provided a new function that enabled image processing inside the device. This was a product that realized new possibilities by taking advantage of the inherent characteristics of 3D stacked semiconductors that combined different types of devices.

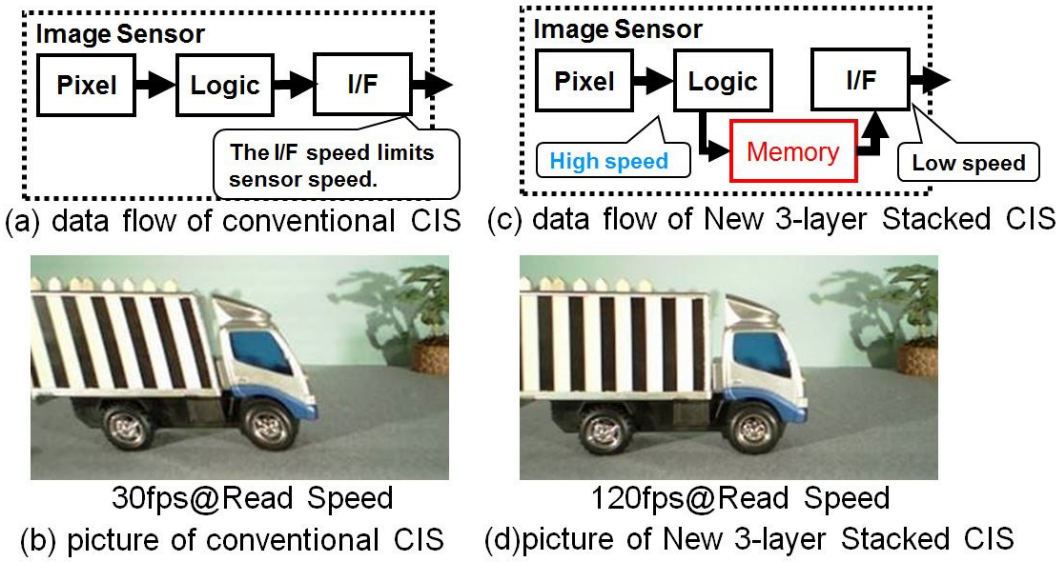

Figure 1 Difference between ordinary CMOS image sensor and triple-layered CMOS image sensor (By courtesy of Sony)

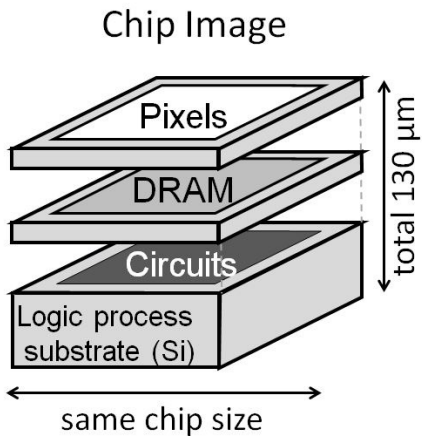

Figure 2 Structure of 3-lyaers stacked CMOS image sensor (By courtesy of Sony)

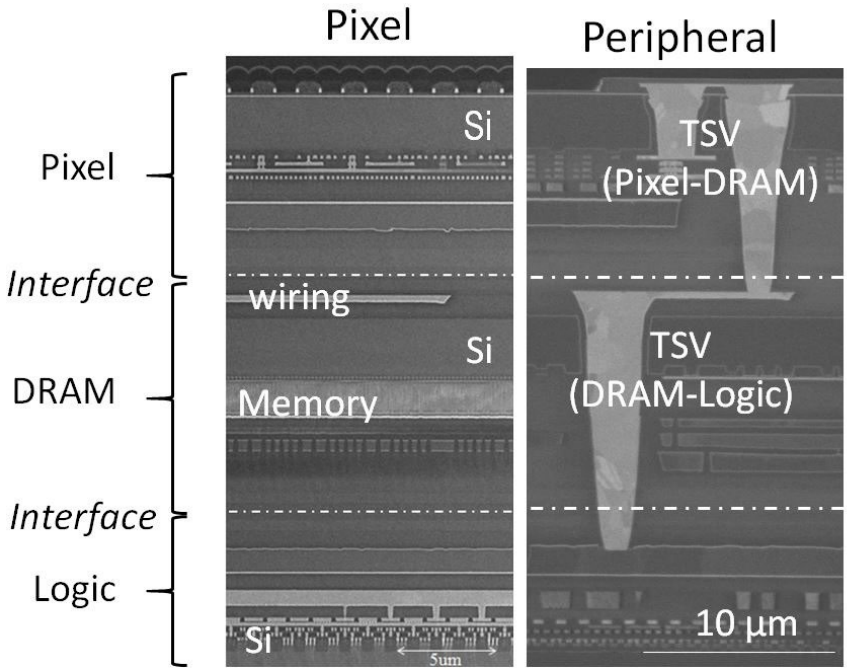

Figure 3　Cross-sectional SEM view of 3-layers stacked CMOS image sensor
(By courtesy of Sony)

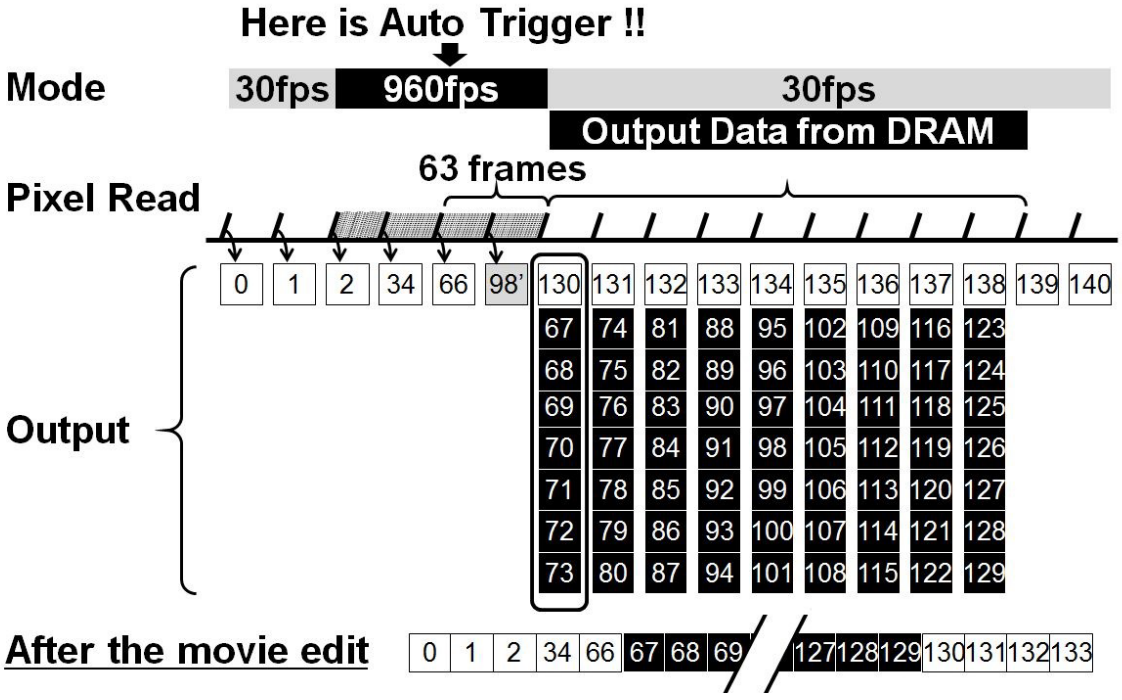

Figure 4　Readout and output sequence in a super slow movie mode
(By courtesy of Sony)

References:

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(2) Taku Umebayashi, “3D Stacked CMOS Image Sensor Exmor RS™”, ISSCC 2014 Forum F2
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(5) Sony New Release, “Sony Develops the Industry's First 3-Layer Stacked CMOS Image Sensor with DRAM for Smartphones”, (February 7, 2017) https://www.sony.com/en/SonyInfo/News/Press/201702/17-013E/

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